

MIXED SIGNAL MICROCONTROLLER

FEATURES

- Low Supply Voltage Range 1.8 V to 3.6 V
- Ultra-Low Power Consumption
 - Active Mode: 365 μ A at 1 MHz, 2.2 V
 - Standby Mode (VLO): 0.5 μ A
 - Off Mode (RAM Retention): 0.1 μ A
- Wake-Up From Standby Mode in Less Than 1 μ s
- 16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time
- Three-Channel Internal DMA
- 12-Bit Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold, and Autoscan Feature
- Dual 12-Bit Digital-to-Analog (D/A) Converters With Synchronization
- 16-Bit Timer_A With Three Capture/Compare Registers
- 16-Bit Timer_B With Seven Capture/Compare-With-Shadow Registers
- On-Chip Comparator
- Four Universal Serial Communication Interfaces (USCIs)
 - USCI_A0 and USCI_A1
 - Enhanced UART Supporting Auto-Baudrate Detection
 - IrDA Encoder and Decoder
 - Synchronous SPI
 - USCI_B0 and USCI_B1
 - I²C™
 - Synchronous SPI
- Supply Voltage Supervisor/Monitor With Programmable Level Detection
- Brownout Detector
- Bootstrap Loader
- Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse
- Family Members:
 - MSP430F2416
 - 92KB + 256B Flash Memory
 - 4KB RAM
 - MSP430F2417
 - 92KB + 256B Flash Memory
 - 8KB RAM
 - MSP430F2418
 - 116KB + 256B Flash Memory
 - 8KB RAM
 - MSP430F2419
 - 120KB + 256B Flash Memory
 - 4KB RAM
 - MSP430F2616
 - 92KB + 256B Flash Memory
 - 4KB RAM
 - MSP430F2617
 - 92KB + 256B Flash Memory
 - 8KB RAM
 - MSP430F2618
 - 116KB + 256B Flash Memory
 - 8KB RAM
 - MSP430F2619
 - 120KB + 256B Flash Memory
 - 4KB RAM
- Available in 80-Pin Quad Flat Pack (LQFP), 64-Pin LQFP, and 113-Pin Ball Grid Array (BGA) (See [Table 1](#))
- For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide* ([SLAU144](#))



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION

The Texas Instruments MSP430 family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The calibrated digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 μ s.

The MSP430F261x and MSP430F241x series are microcontroller configurations with two built-in 16-bit timers, a fast 12-bit A/D converter, a comparator, dual 12-bit D/A converters, four universal serial communication interface (USCI) modules, DMA, and up to 64 I/O pins. The MSP430F241x devices are identical to the MSP430F261x devices, with the exception that the DAC12 and the DMA modules are not implemented.

Typical applications include sensor systems, industrial control applications, and hand-held meters. The 12mmx12mm LQFP-64 package is also available as a non-magnetic package for medical imaging applications.

Table 1. Available Options⁽¹⁾

| T _A | PACKAGED DEVICES ⁽²⁾ | | |
|----------------|--|--|--|
| | PLASTIC 113-PIN BGA (ZQW) | PLASTIC 80-PIN LQFP (PN) | PLASTIC 64-PIN LQFP (PM) |
| -40°C to 105°C | MSP430F2416TZQW MSP430F2417TZQW MSP430F2418TZQW MSP430F2419TZQW MSP430F2616TZQW MSP430F2617TZQW MSP430F2618TZQW MSP430F2619TZQW | MSP430F2416TPN MSP430F2417TPN MSP430F2418TPN MSP430F2419TPN MSP430F2616TPN MSP430F2617TPN MSP430F2618TPN MSP430F2619TPN | MSP430F2416TPM MSP430F2417TPM MSP430F2418TPM MSP430F2419TPM MSP430F2616TPM MSP430F2617TPM MSP430F2618TPM MSP430F2619TPM MSP430F2618TPMR-NM |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

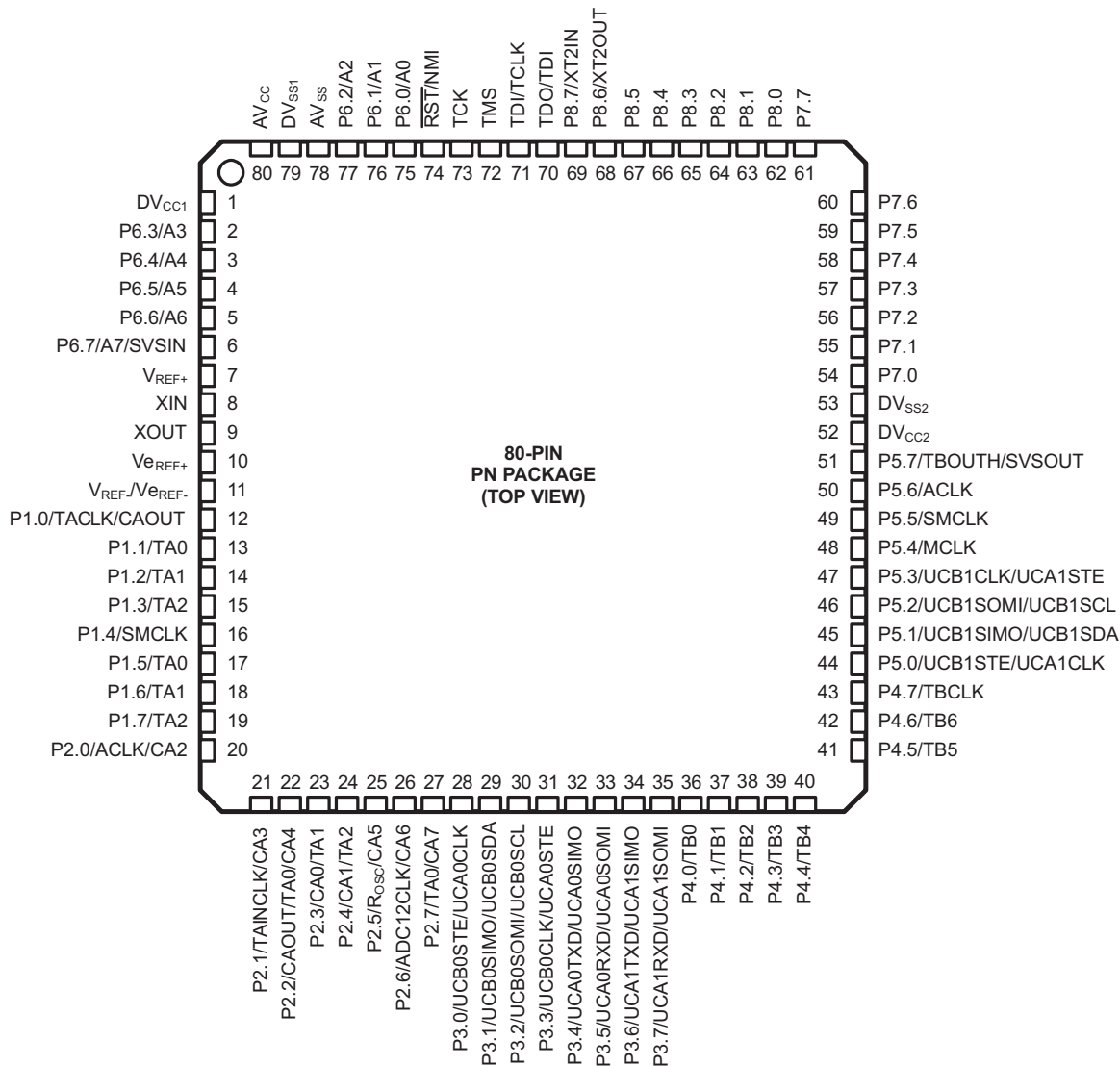
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Development Tool Support

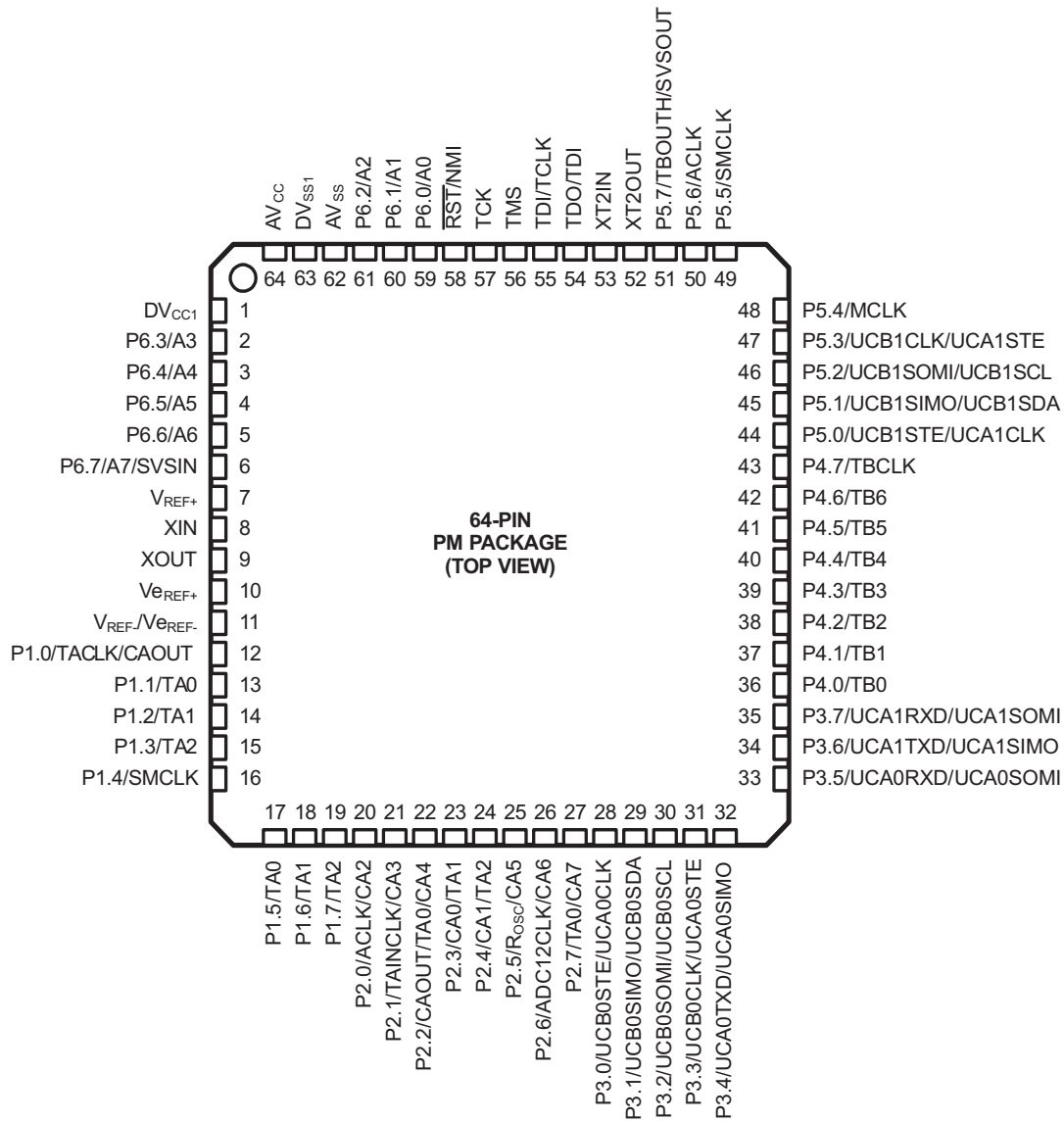
All MSP430 microcontrollers include an Embedded Emulation Module (EEM) allowing advanced debugging and programming through easy-to-use development tools. Recommended hardware options include:

- Debugging and Programming Interface
 - MSP-FET430UIF (USB)
 - MSP-FET430PIF (Parallel Port)
- Debugging and Programming Interface with Target Board
 - MSP-FET430U64 (PM Package)
 - MSP-FET430U80 (PN Package)
- Standalone Target Board
 - MSP-TS430PM64
- Production Programmer
 - MSP-GANG430

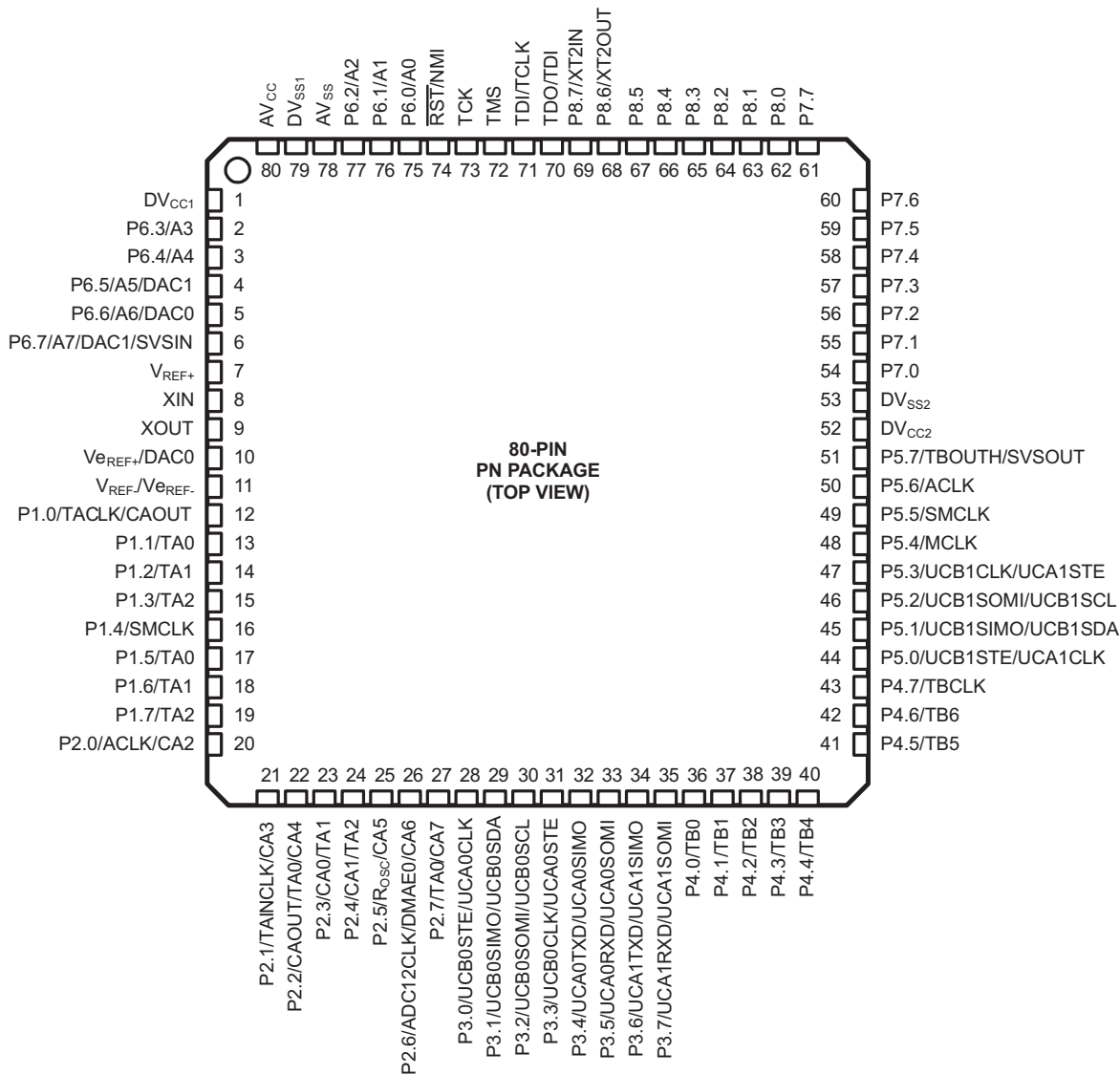
Device Pinout, MSP430F241x, 80-Pin PN Package



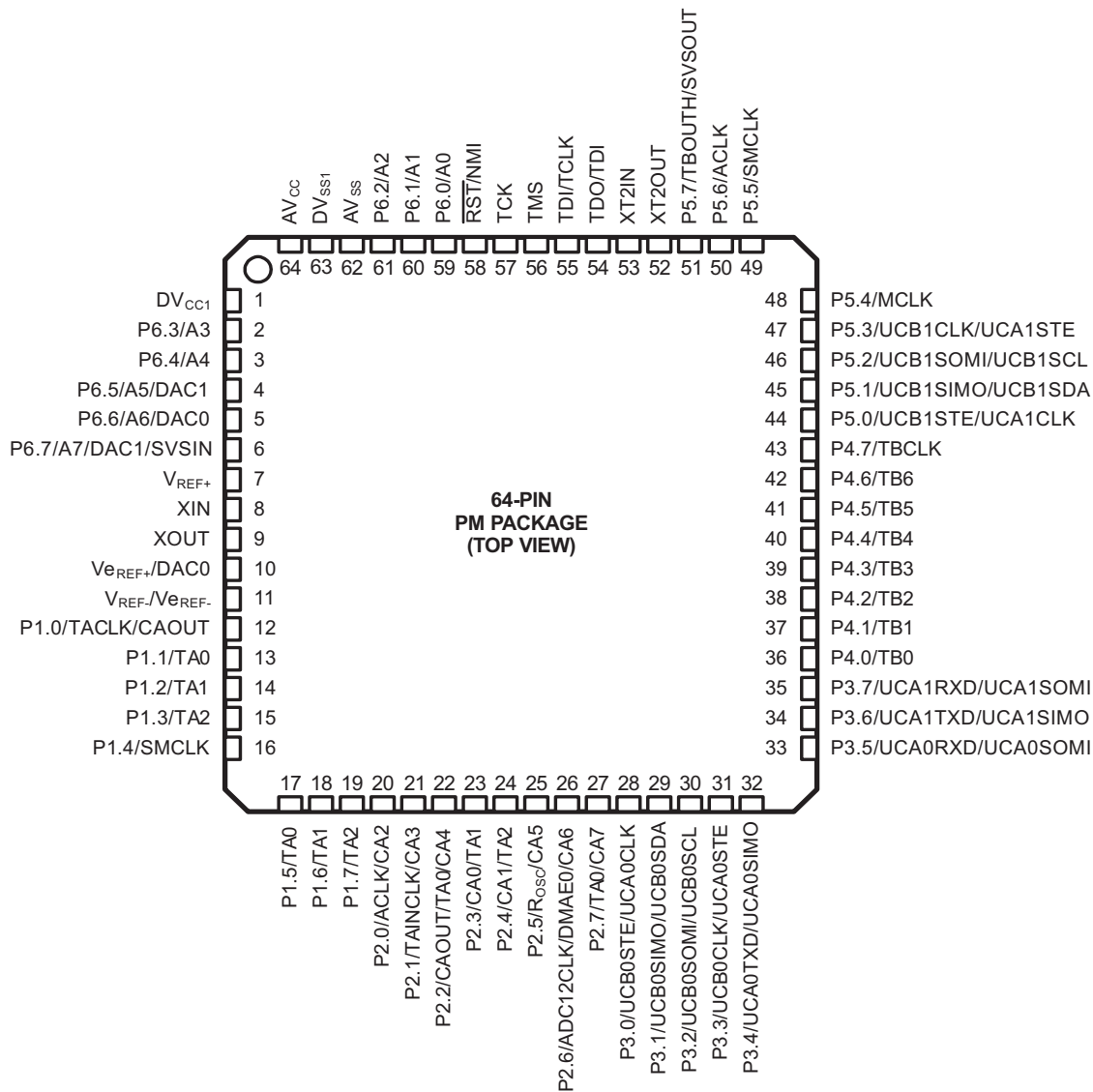
Device Pinout, MSP430F241x, 64-Pin PM Package



Device Pinout, MSP430F261x, 80-Pin PN Package



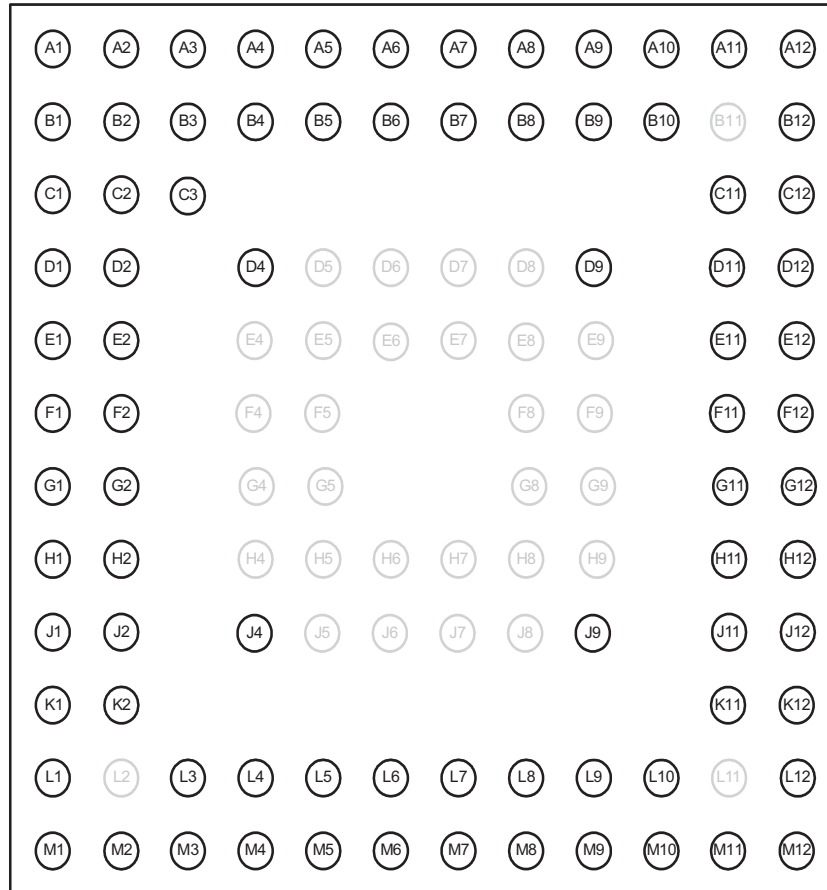
Device Pinout, MSP430F261x, 64-Pin PM Package



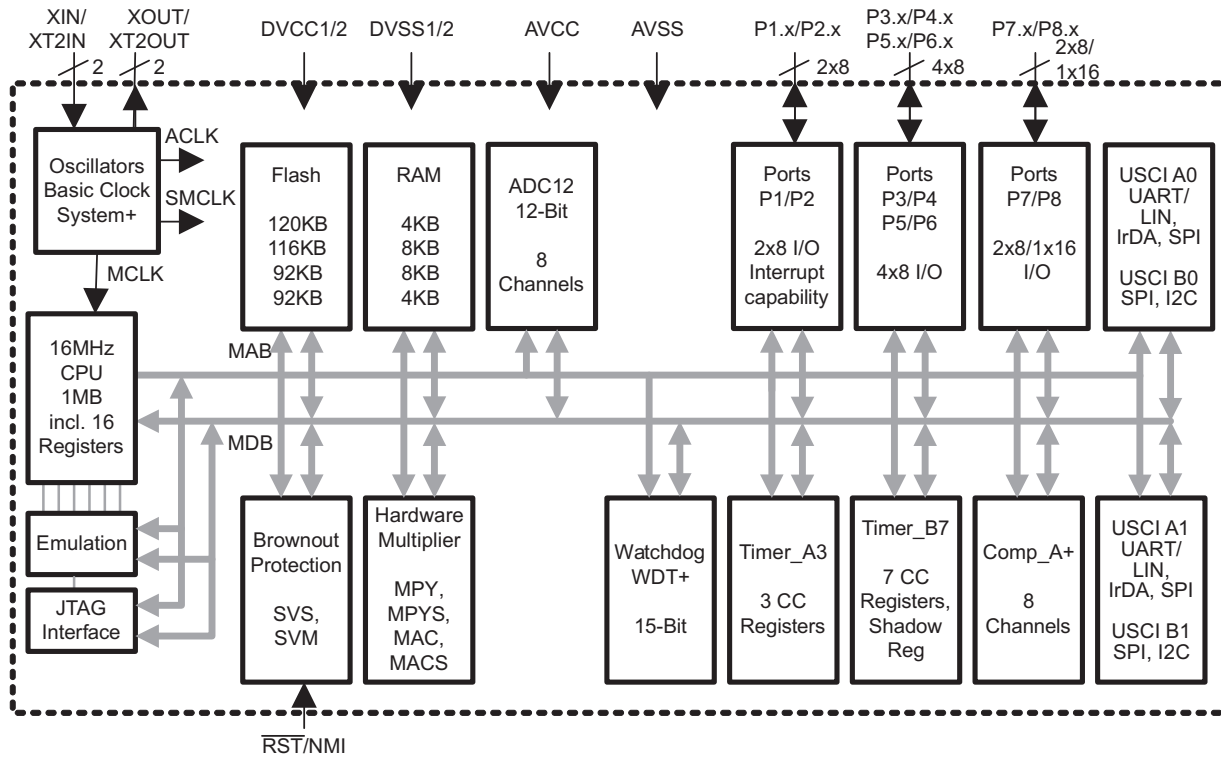
Device Pinout, 113-Pin ZQW Package

NOTE

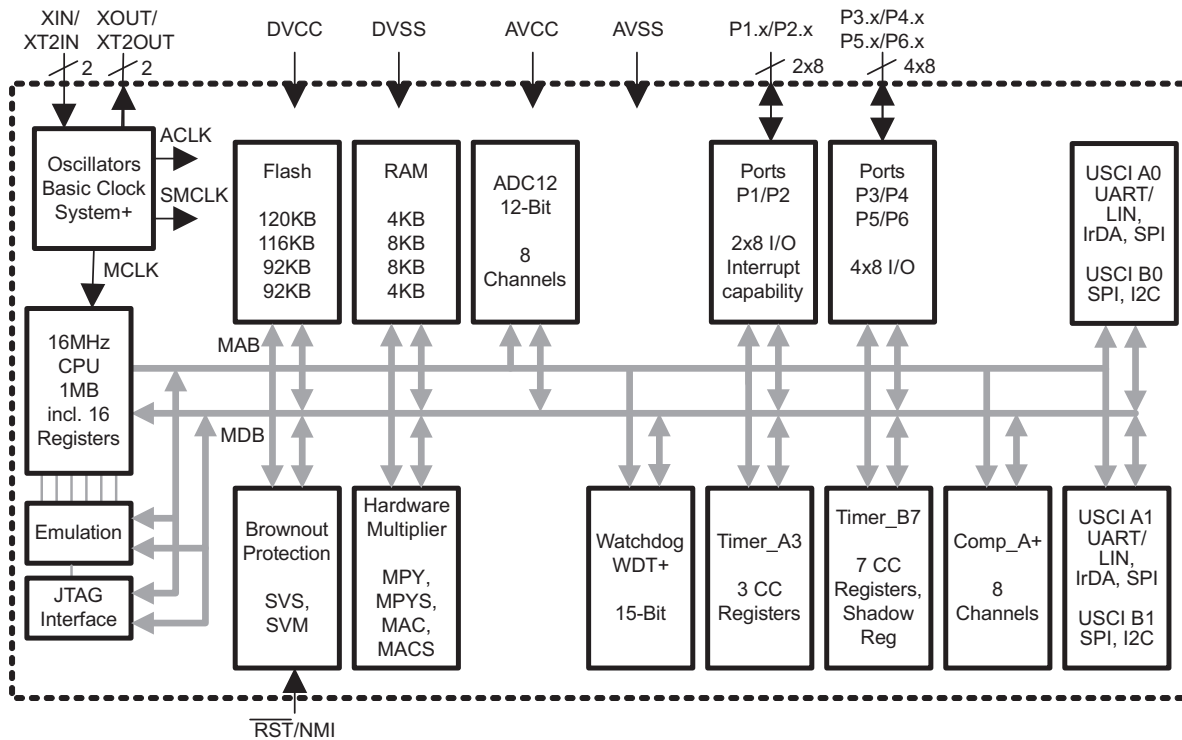
For terminal assignments, see [Table 2](#).



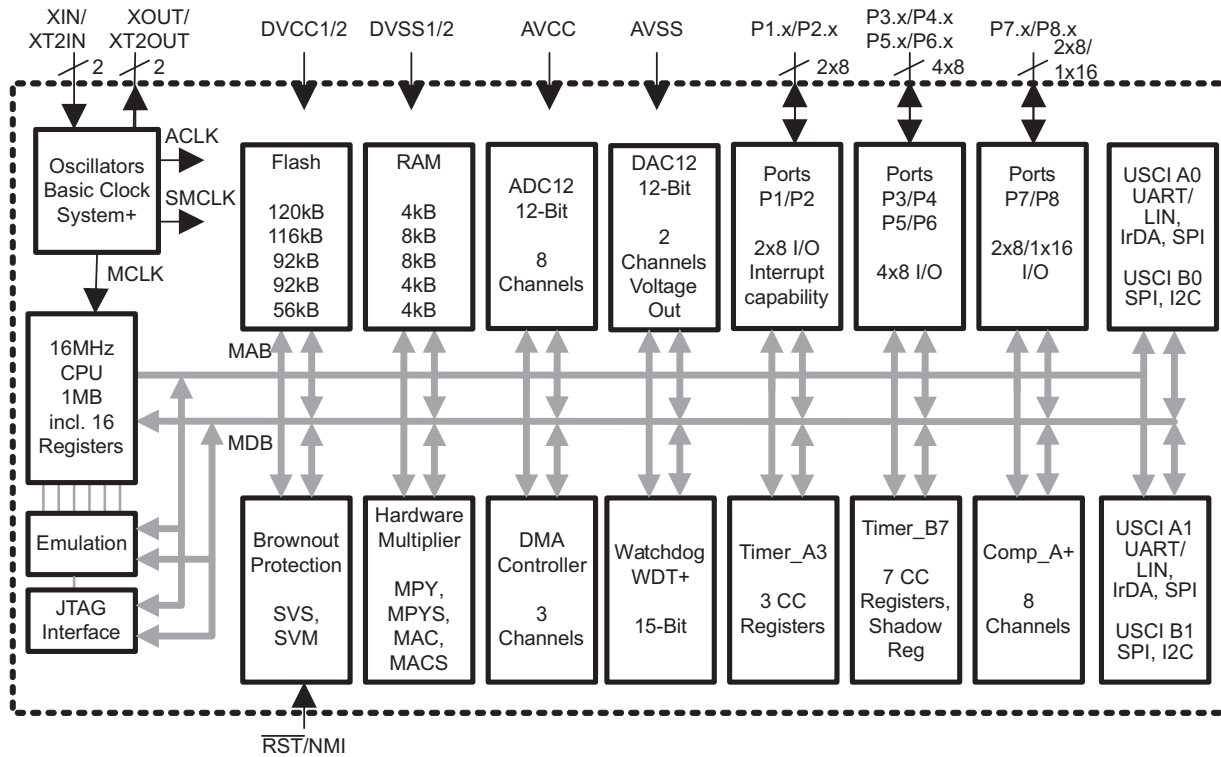
Functional Block Diagram, MSP430F241x, 80-Pin PN Package



Functional Block Diagram, MSP430F241x, 64-Pin PM Package



Functional Block Diagram, MSP430F261x, 80-Pin PN Package



Functional Block Diagram, MSP430F261x, 64-Pin PM Package

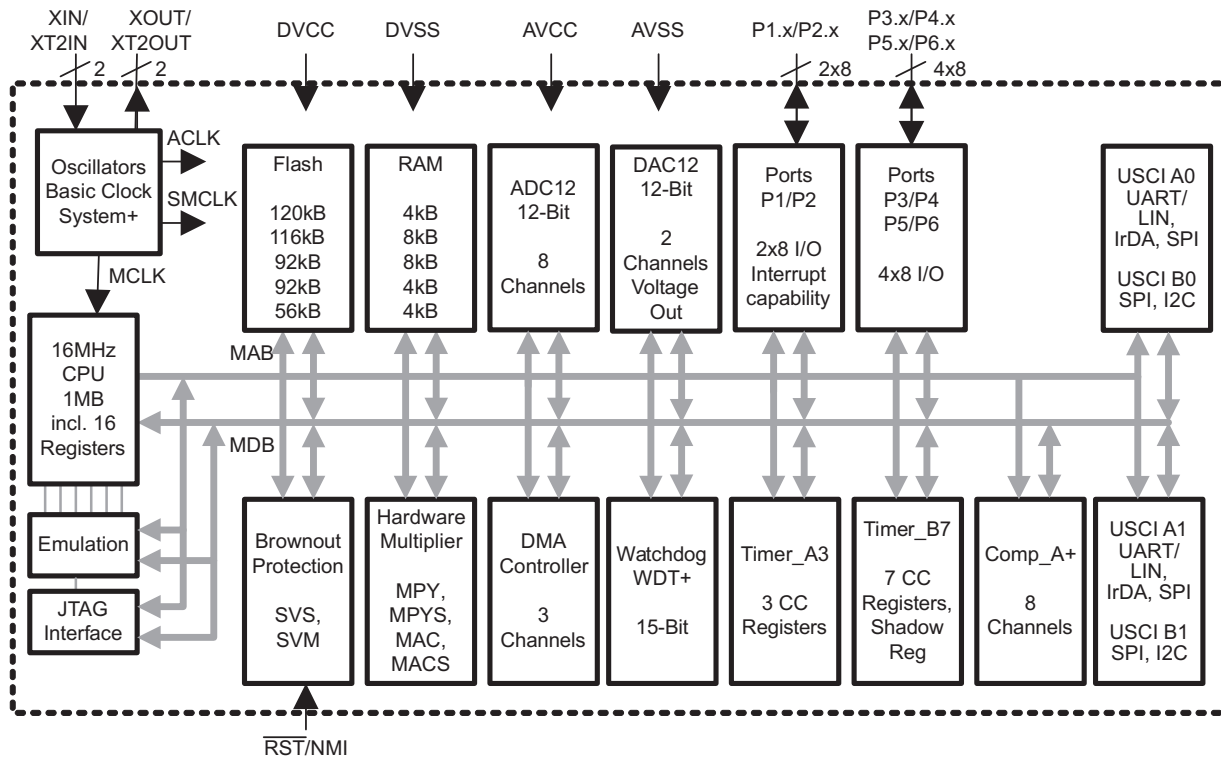


Table 2. Terminal Functions

| TERMINAL | | | | I/O | DESCRIPTION |
|----------------------------|--------|--------|---------|-----|--|
| NAME | NO. | | | | |
| | 64 PIN | 80 PIN | 113 PIN | | |
| AV _{CC} | 64 | 80 | A2 | | Analog supply voltage, positive terminal. Supplies only the analog portion of ADC12 and DAC12. |
| AV _{SS} | 62 | 78 | B2, B3 | | Analog supply voltage, negative terminal. Supplies only the analog portion of ADC12 and DAC12. |
| DV _{CC1} | 1 | 1 | A1 | | Digital supply voltage, positive terminal. Supplies all digital parts. |
| DV _{SS1} | 63 | 79 | A3 | | Digital supply voltage, negative terminal. Supplies all digital parts. |
| DV _{CC2} | | 52 | F12 | | Digital supply voltage, positive terminal. Supplies all digital parts. |
| DV _{SS2} | | 53 | E12 | | Digital supply voltage, negative terminal. Supplies all digital parts. |
| P1.0/TACLK/CAOUT | 12 | 12 | G2 | I/O | General-purpose digital I/O pin Timer_A, clock signal TACLK input Comparator_A output |
| P1.1/TA0 | 13 | 13 | H1 | I/O | General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: Out0 output BSL transmit |
| P1.2/TA1 | 14 | 14 | H2 | I/O | General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare: Out1 output |
| P1.3/TA2 | 15 | 15 | J1 | I/O | General-purpose digital I/O pin Timer_A, capture: CCI2A input, compare: Out2 output |
| P1.4/SMCLK | 16 | 16 | J2 | I/O | General-purpose digital I/O pin SMCLK signal output |
| P1.5/TA0 | 17 | 17 | K1 | I/O | General-purpose digital I/O pin Timer_A, compare: Out0 output |
| P1.6/TA1 | 18 | 18 | K2 | I/O | General-purpose digital I/O pin Timer_A, compare: Out1 output |
| P1.7/TA2 | 19 | 19 | L1 | I/O | General-purpose digital I/O pin Timer_A, compare: Out2 output |
| P2.0/ACLK/CA2 | 20 | 20 | M1 | I/O | General-purpose digital I/O pin ACLK output/Comparator_A input |
| P2.1/TAINCLK/CA3 | 21 | 21 | M2 | I/O | General-purpose digital I/O pin Timer_A, clock signal at INCLK |
| P2.2/CAOUT/TA0/CA4 | 22 | 22 | M3 | I/O | General-purpose digital I/O pin Timer_A, capture: CCI0B input Comparator_A output BSL receive Comparator_A input |
| P2.3/CA0/TA1 | 23 | 23 | L3 | I/O | General-purpose digital I/O pin Timer_A, compare: Out1 output Comparator_A input |
| P2.4/CA1/TA2 | 24 | 24 | L4 | I/O | General-purpose digital I/O pin Timer_A, compare: Out2 output Comparator_A input |
| P2.5/R _{OSC} /CA5 | 25 | 25 | M4 | I/O | General-purpose digital I/O pin Input for external resistor defining the DCO nominal frequency Comparator_A input |

Table 2. Terminal Functions (continued)

| TERMINAL | | | | I/O | DESCRIPTION |
|---|--------|--------|---------|-----|--|
| NAME | NO. | | | | |
| | 64 PIN | 80 PIN | 113 PIN | | |
| P2.6/ADC12CLK/ DMAE0 ⁽¹⁾ /CA6 | 26 | 26 | J4 | I/O | General-purpose digital I/O pin Conversion clock - 12-bit ADC DMA channel 0 external trigger Comparator_A input |
| P2.7/TA0/CA7 | 27 | 27 | L5 | I/O | General-purpose digital I/O pin Timer_A, compare: Out0 output Comparator_A input |
| P3.0/UCB0STE/ UCA0CLK | 28 | 28 | M5 | I/O | General-purpose digital I/O pin USCI_B0 slave transmit enable/USCI_A0 clock input/output |
| P3.1/UCB0SIMO/ UCB0SDA | 29 | 29 | L6 | I/O | General-purpose digital I/O pin USCI_B0 slave-in master-out in SPI mode, SDA I2C data in I2C mode |
| P3.2/UCB0SOMI/ UCB0SCL | 30 | 30 | M6 | I/O | General-purpose digital I/O pin USCI_B0 slave-out master-in in SPI mode, SCL I2C clock in I2C mode |
| P3.3/UCB0CLK/ UCA0STE | 31 | 31 | L7 | I/O | General-purpose digital I/O USCI_B0 clock input/output, USCI_A0 slave transmit enable |
| P3.4/UCA0TXD/ UCA0SIMO | 32 | 32 | M7 | I/O | General-purpose digital I/O pin USCI_A transmit data output in UART mode, slave data in/master out in SPI mode |
| P3.5/UCA0RXD/ UCA0SOMI | 33 | 33 | L8 | I/O | General-purpose digital I/O pin USCI_A0 receive data input in UART mode, slave data out/master in in SPI mode |
| P3.6/UCA1TXD/ UCA1SIMO | 34 | 34 | M8 | I/O | General-purpose digital I/O pin USCI_A1 transmit data output in UART mode, slave data in/master out in SPI mode |
| P3.7/UCA1RXD/ UCA1SOMI | 35 | 35 | L9 | I/O | General-purpose digital I/O pin USCI_A1 receive data input in UART mode, slave data out/master in in SPI mode |
| P4.0/TB0 | 36 | 36 | M9 | I/O | General-purpose digital I/O pin Timer_B, capture: CCI0A/B input, compare: Out0 output |
| P4.1/TB1 | 37 | 37 | J9 | I/O | General-purpose digital I/O pin Timer_B, capture: CCI1A/B input, compare: Out1 output |
| P4.2/TB2 | 38 | 38 | M10 | I/O | General-purpose digital I/O pin Timer_B, capture: CCI2A/B input, compare: Out2 output |
| P4.3/TB3 | 39 | 39 | L10 | I/O | General-purpose digital I/O pin Timer_B, capture: CCI3A/B input, compare: Out3 output |
| P4.4/TB4 | 40 | 40 | M11 | I/O | General-purpose digital I/O pin Timer_B, capture: CCI4A/B input, compare: Out4 output |
| P4.5/TB5 | 41 | 41 | M12 | I/O | General-purpose digital I/O pin Timer_B, capture: CCI5A/B input, compare: Out5 output |
| P4.6/TB6 | 42 | 42 | L12 | I/O | General-purpose digital I/O pin Timer_B, capture: CCI6A input, compare: Out6 output |
| P4.7/TBCLK | 43 | 43 | K11 | I/O | General-purpose digital I/O pin Timer_B, clock signal TBCLK input |

(1) MSP430F261x devices only

Table 2. Terminal Functions (continued)

| TERMINAL | | | | I/O | DESCRIPTION |
|------------------------------------|--------|--------|-----------|-----|--|
| NAME | NO. | | | | |
| | 64 PIN | 80 PIN | 113 PIN | | |
| P5.0/UCB1STE/ UCA1CLK | 44 | 44 | K12 | I/O | General-purpose digital I/O pin USCI_B1 slave transmit enable/USCI_A1 clock input/output |
| P5.1/UCB1SIMO/ UCB1SDA | 45 | 45 | J11 | I/O | General-purpose digital I/O pin USCI_B1 slave-in master-out in SPI mode, SDA I2C data in I2C mode |
| P5.2/UCB1SOMI/ UCB1SCL | 46 | 46 | J12 | I/O | General-purpose digital I/O pin USCI_B1 slave-out master-in in SPI mode, SCL I2C clock in I2C mode |
| P5.3/UCB1CLK/ UCA1STE | 47 | 47 | H11 | I/O | General-purpose digital I/O USCI_B1 clock input/output, USCI_A1 slave transmit enable |
| P5.4/MCLK | 48 | 48 | H12 | I/O | General-purpose digital I/O pin Main system clock MCLK output |
| P5.5/SMCLK | 49 | 49 | G11 | I/O | General-purpose digital I/O pin Submain system clock SMCLK output |
| P5.6/ACLK | 50 | 50 | G12 | I/O | General-purpose digital I/O pin Auxiliary clock ACLK output |
| P5.7/TBOUTH/SVSOUT | 51 | 51 | F11 | I/O | General-purpose digital I/O pin Switch all PWM digital output ports to high impedance - Timer_B TB0 to TB6 SVS comparator output |
| P6.0/A0 | 59 | 75 | D4 | I/O | General-purpose digital I/O pin Analog input A0 - 12-bit ADC |
| P6.1/A1 | 60 | 76 | A4 | I/O | General-purpose digital I/O pin Analog input A1 - 12-bit ADC |
| P6.2/A2 | 61 | 77 | B4 | I/O | General-purpose digital I/O pin Analog input A2 - 12-bit ADC |
| P6.3/A3 | 2 | 2 | B1 | I/O | General-purpose digital I/O pin Analog input A3 - 12-bit ADC |
| P6.4/A4 | 3 | 3 | C1 | I/O | General-purpose digital I/O pin Analog input A4 - 12-bit ADC |
| P6.5/A5/DAC1 ⁽²⁾ | 4 | 4 | C2, C3 | I/O | General-purpose digital I/O pin Analog input A5 - 12-bit ADC DAC12.1 output |
| P6.6/A6/DAC0 ⁽²⁾ | 5 | 5 | D1 | I/O | General-purpose digital I/O pin Analog input A6 - 12-bit ADC DAC12.0 output |
| P6.7/A7/DAC1 ⁽²⁾ /SVSIN | 6 | 6 | D2 | I/O | General-purpose digital I/O pin Analog input A7 - 12-bit ADC DAC12.1 output SVS input |
| P7.0 | | 54 | E11 | I/O | General-purpose digital I/O pin |
| P7.1 | | 55 | D12 | I/O | General-purpose digital I/O pin |
| P7.2 | | 56 | D11 | I/O | General-purpose digital I/O pin |
| P7.3 | | 57 | C12 | I/O | General-purpose digital I/O pin |
| P7.4 | | 58 | C11 | I/O | General-purpose digital I/O pin |

(2) MSP430F261x devices only

Table 2. Terminal Functions (continued)

| TERMINAL | | | | I/O | DESCRIPTION |
|--|--------|--------|----------------|-----|---|
| NAME | NO. | | | | |
| | 64 PIN | 80 PIN | 113 PIN | | |
| P7.5 | | 59 | B12 | I/O | General-purpose digital I/O pin |
| P7.6 | | 60 | A12 | I/O | General-purpose digital I/O pin |
| P7.7 | | 61 | A11 | I/O | General-purpose digital I/O pin |
| P8.0 | | 62 | B10 | I/O | General-purpose digital I/O pin |
| P8.1 | | 63 | A10 | I/O | General-purpose digital I/O pin |
| P8.2 | | 64 | D9 | I/O | General-purpose digital I/O pin |
| P8.3 | | 65 | A9 | I/O | General-purpose digital I/O pin |
| P8.4 | | 66 | B9 | I/O | General-purpose digital I/O pin |
| P8.5 | | 67 | B8 | I/O | General-purpose digital I/O pin |
| P8.6/XT2OUT | | 68 | A8 | I/O | General-purpose digital I/O pin Output terminal of crystal oscillator XT2 |
| P8.7/XT2IN | | 69 | A7 | I/O | General-purpose digital I/O pin Input port for crystal oscillator XT2. Only standard crystals can be connected. |
| XT2OUT | 52 | | | O | Output terminal of crystal oscillator XT2 |
| XT2IN | 53 | | | I | Input port for crystal oscillator XT2 |
| RST/NMI | 58 | 74 | B5 | I | Reset input, nonmaskable interrupt input port, or bootstrap loader start (in flash devices) |
| TCK | 57 | 73 | A5 | I | Test clock (JTAG). TCK is the clock input port for device programming test and bootstrap loader start |
| TDI/TCLK | 55 | 71 | A6 | I | Test data input or test clock input. The device protection fuse is connected to TDI/TCLK. |
| TDO/TDI | 54 | 70 | B7 | I/O | Test data output port. TDO/TDI data output or programming data input terminal. |
| TMS | 56 | 72 | B6 | I | Test mode select. TMS is used as an input port for device programming and test. |
| V _{REF+} /DAC0 ⁽³⁾ | 10 | 10 | F2 | I | Input for an external reference voltage/DAC12.0 output |
| V _{REF+} | 7 | 7 | E2 | O | Output of positive terminal of the reference voltage in the ADC12 |
| V _{REF-} /V _{REF-} | 11 | 11 | G1 | I | Negative terminal for the reference voltage for both sources, the internal reference voltage or an external applied reference voltage |
| XIN | 8 | 8 | E1 | I | Input port for crystal oscillator XT1. Standard or watch crystals can be connected. |
| XOUT | 9 | 9 | F1 | O | Output port for crystal oscillator XT1. Standard or watch crystals can be connected. |
| Reserved | - | - | ⁽⁴⁾ | NA | Reserved pins. Connection to DV _{SS} , AV _{SS} recommended. |

(3) MSP430F261x devices only

(4) Reserved pins are L2, E4, F4, G4, H4, D5, E5, F5, G5, H5, J5, D6, E6, H6, J6, D7, E7, H7, J7, D8, E8, F8, G8, H8, J8, E9, F9, G9, H9, B11, L11.

SHORT-FORM DESCRIPTION

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. [Table 3](#) shows examples of the three types of instruction formats; [Table 4](#) shows the address modes.

| | |
|--------------------------|-----------|
| Program Counter | PC/R0 |
| Stack Pointer | SP/R1 |
| Status Register | SR/CG1/R2 |
| Constant Generator | CG2/R3 |
| General-Purpose Register | R4 |
| General-Purpose Register | R5 |
| General-Purpose Register | R6 |
| General-Purpose Register | R7 |
| General-Purpose Register | R8 |
| General-Purpose Register | R9 |
| General-Purpose Register | R10 |
| General-Purpose Register | R11 |
| General-Purpose Register | R12 |
| General-Purpose Register | R13 |
| General-Purpose Register | R14 |
| General-Purpose Register | R15 |

Table 3. Instruction Word Formats

| INSTRUCTION FORMAT | EXAMPLE | OPERATION |
|-----------------------------------|-----------|-----------------------|
| Dual operands, source-destination | ADD R4,R5 | R4 + R5 -> R5 |
| Single operands, destination only | CALL R8 | PC ->(TOS), R8-> PC |
| Relative jump, un/conditional | JNE | Jump-on-equal bit = 0 |

Table 4. Address Mode Descriptions

| ADDRESS MODE | S ⁽¹⁾ | D ⁽¹⁾ | SYNTAX | EXAMPLE | OPERATION |
|------------------------|------------------|------------------|-----------------|------------------|--------------------------------|
| Register | ✓ | ✓ | MOV Rs,Rd | MOV R10,R11 | R10 -> R11 |
| Indexed | ✓ | ✓ | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6) | M(2+R5)-> M(6+R6) |
| Symbolic (PC relative) | ✓ | ✓ | MOV EDE,TONI | | M(EDE) -> M(TONI) |
| Absolute | ✓ | ✓ | MOV &MEM,&TCDAT | | M(MEM) -> M(TCDAT) |
| Indirect | ✓ | | MOV @Rn,Y(Rm) | MOV @R10,Tab(R6) | M(R10) -> M(Tab+R6) |
| Indirect autoincrement | ✓ | | MOV @Rn+,Rm | MOV @R10+,R11 | M(R10) -> R11 R10 + 2-> R10 |
| Immediate | ✓ | | MOV #X,TONI | MOV #45,TONI | #45 -> M(TONI) |

(1) S = source, D = destination

Operating Modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
 - All clocks are active
- Low-power mode 0 (LPM0)
 - CPU is disabled
 - ACLK and SMCLK remain active
 - MCLK is disabled
- Low-power mode 1 (LPM1)
 - CPU is disabled
 - ACLK and SMCLK remain active. MCLK is disabled
 - DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
 - CPU is disabled
 - MCLK and SMCLK are disabled
 - DCO's dc-generator remains enabled
 - ACLK remains active
- Low-power mode 3 (LPM3)
 - CPU is disabled
 - MCLK and SMCLK are disabled
 - DCO's dc-generator is disabled
 - ACLK remains active
- Low-power mode 4 (LPM4)
 - CPU is disabled
 - ACLK is disabled
 - MCLK and SMCLK are disabled
 - DCO's dc-generator is disabled
 - Crystal oscillator is stopped

Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range of 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (for example, flash is not programmed) the CPU enters LPM4 immediately after power-up.

Table 5. Interrupt Sources

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|--|--|---|------------------|-----------------|
| Power-up External reset Watchdog Timer+ Flash key violation PC out-of-range ⁽¹⁾ | PORIFG RSTIFG WDTIFG KEYV See ⁽²⁾ | Reset | 0FFFEh | 31, highest |
| NMI Oscillator fault Flash memory access violation | NMIIFG OFIFG ACCVIFG ⁽²⁾⁽³⁾ | (Non)maskable, (Non)maskable, (Non)maskable | 0FFFCh | 30 |
| Timer_B7 | TBCCR0 CCIFG ⁽⁴⁾ | Maskable | 0FFFAh | 29 |
| Timer_B7 | TBCCR1 to TBCCR6 CCIFGs, TBIFG ⁽²⁾⁽⁴⁾ | Maskable | 0FFF8h | 28 |
| Comparator_A+ | CAIFG | Maskable | 0FFF6h | 27 |
| Watchdog Timer+ | WDTIFG | Maskable | 0FFF4h | 26 |
| Timer_A3 | TACCR0 CCIFG ⁽⁴⁾ | Maskable | 0FFF2h | 25 |
| Timer_A3 | TACCR1 CCIFG TACCR2 CCIFG ⁽²⁾⁽⁴⁾ | Maskable | 0FFF0h | 24 |
| USCI_A0/USCI_B0 receive USCI_B0 I2C status | UCA0RXIFG, UCB0RXIFG ⁽²⁾⁽⁵⁾ | Maskable | 0FFEEh | 23 |
| USCI_A0/USCI_B0 transmit USCI_B0 I2C receive or transmit | UCA0TXIFG, UCB0TXIFG ⁽²⁾⁽⁶⁾ | Maskable | 0FFECh | 22 |
| ADC12 | ADC12IFG ⁽²⁾⁽⁴⁾ | Maskable | 0FFEAh | 21 |
| | | | 0FFE8h | 20 |
| I/O port P2 (eight flags) | P2IFG.0 to P2IFG.7 ⁽²⁾⁽⁴⁾ | Maskable | 0FFE6h | 19 |
| I/O port P1 (eight flags) | P1IFG.0 to P1IFG.7 ⁽²⁾⁽⁴⁾ | Maskable | 0FFE4h | 18 |
| USCI_A1/USCI_B1 receive USCI_B1 I2C status | UCA1RXIFG, UCB1RXIFG ⁽²⁾⁽⁵⁾ | Maskable | 0FFE2h | 17 |
| USCI_A1/USCI_B1 transmit USCI_B1 I2C receive or transmit | UCA1TXIFG, UCB1TXIFG ⁽²⁾⁽⁶⁾ | Maskable | 0FFE0h | 16 |
| DMA | DMA0IFG, DMA1IFG, DMA2IFG ⁽²⁾⁽⁴⁾ | Maskable | 0FFDEh | 15 |
| DAC12 | DAC12_0IFG, DAC12_1IFG ⁽²⁾⁽⁴⁾ | Maskable | 0FFDCh | 14 |
| See ⁽⁷⁾⁽⁸⁾ | | | 0FFDAh to 0FFC0h | 15 to 0, lowest |

- (1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
- (2) Multiple source flags
- (3) (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
- (4) Interrupt flags are located in the module.
- (5) In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG.
- (6) In UART/SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, UCB0TXIFG.
- (7) The address 0FFBEh is used as bootstrap loader security key (BSLSKEY).
A 0AA55h at this location disables the BSL completely.
A zero disables the erasure of the flash if an invalid password is supplied.
- (8) The interrupt vectors at addresses 0FFDAh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

Special Function Registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.










| | | |
|---------------|---|---|
| Legend | rw: | Bit can be read and written. |
| | rw-0,1: | Bit can be read and written. It is reset or set by PUC. |
| | rw-(0,1): | Bit can be read and written. It is reset or set by POR. |
| |  | SFR bit is not present in device. |

Table 6. Interrupt Enable Register 1 and 2




| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---------------|--------------|--|---|-------------|--------------|
| 00h |  |  | ACCVIE | NMIIE |  |  | OFIE | WDTIE |
| | | | rw-0 | rw-0 | | | rw-0 | rw-0 |

| | |
|---------------|--|
| WDTIE | Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode. |
| OFIE | Oscillator fault interrupt enable |
| NMIIE | (Non)maskable interrupt enable |
| ACCVIE | Flash access violation interrupt enable |





| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|-----------------|-----------------|-----------------|-----------------|
| 01h |  |  |  |  | UCB0TXIE | UCB0RXIE | UCA0TXIE | UCA0RXIE |
| | | | | | rw-0 | rw-0 | rw-0 | rw-0 |

| | |
|-----------------|-----------------------------------|
| UCA0RXIE | USCI_A0 receive interrupt enable |
| UCA0TXIE | USCI_A0 transmit interrupt enable |
| UCB0RXIE | USCI_B0 receive interrupt enable |
| UCB0TXIE | USCI_B0 transmit interrupt enable |

Table 7. Interrupt Flag Register 1 and 2

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---------------|---------------|---------------|--------------|---------------|
| 02h |  |  |  | NMIIFG | RSTIFG | PORIFG | OFIFG | WDTIFG |
| | | | | rw-0 | rw-(0) | rw-(1) | rw-1 | rw-(0) |

| | |
|---------------|--|
| WDTIFG | Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V _{CC} power-on or a reset condition at the $\overline{\text{RST}}$ /NMI pin in reset mode. |
| OFIFG | Flag set on oscillator fault. |
| PORIFG | Power-On Reset interrupt flag. Set on V _{CC} power-up. |
| RSTIFG | External reset interrupt flag. Set on a reset condition at $\overline{\text{RST}}$ /NMI pin in reset mode. Reset on V _{CC} power-up. |
| NMIIFG | Set via $\overline{\text{RST}}$ /NMI pin |

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------------------|------------------|------------------|------------------|
| 03h |  |  |  |  | UCB0TXIFG | UCB0RXIFG | UCA0TXIFG | UCA0RXIFG |
| | | | | | rw-1 | rw-0 | rw-1 | rw-0 |

| | |
|------------------|---------------------------------|
| UCA0RXIFG | USCI_A0 receive interrupt flag |
| UCA0TXIFG | USCI_A0 transmit interrupt flag |
| UCB0RXIFG | USCI_B0 receive interrupt flag |
| UCB0TXIFG | USCI_B0 transmit interrupt flag |

Memory Organization

Table 8. Memory Organization

| | | MSP430F2416 MSP430F2616 | MSP430F2417 MSP430F2617 | MSP430F2418 MSP430F2618 | MSP430F2419 MSP430F2619 |
|-------------------------------------|-----------|----------------------------|----------------------------|----------------------------|----------------------------|
| Memory | Size | 92KB | 92KB | 116KB | 120KB |
| Main: interrupt vector | Flash | 0x0FFFF-0x0FFC0 | 0x0FFFF-0x0FFC0 | 0x0FFFF-0x0FFC0 | 0x0FFFF-0x0FFC0 |
| Main: code memory | Flash | 0x18FFF-0x02100 | 0x19FFF-0x03100 | 0x1FFFF-0x03100 | 0x1FFFF-0x02100 |
| RAM (total) | Size | 4KB 0x020FF-0x01100 | 8KB 0x030FF-0x01100 | 8KB 0x030FF-0x01100 | 4KB 0x020FF-0x01100 |
| Extended | Size | 2KB 0x020FF-0x01900 | 6KB 0x030FF-0x01900 | 6KB 0x030FF-0x01900 | 2KB 0x020FF-0x01900 |
| Mirrored | Size | 2KB 0x018FF-0x01100 | 2KB 0x018FF-0x01100 | 2KB 0x018FF-0x01100 | 2KB 0x018FF-0x01100 |
| Information memory | Size | 256 Byte | 256 Byte | 256 Byte | 256 Byte |
| | Flash | 0x010FF-0x01000 | 0x010FF-0x01000 | 0x010FF-0x01000 | 0x010FF-0x01000 |
| Boot memory | Size | 1KB | 1KB | 1KB | 1KB |
| | ROM | 0x00FFF-0x00C00 | 0x00FFF-0x00C00 | 0x00FFF-0x00C00 | 0x00FFF-0x00C00 |
| RAM (mirrored at 0x18FF to 0x01100) | Size | 2KB 0x009FF-0x00200 | 2KB 0x009FF-0x00200 | 2KB 0x009FF-0x00200 | 2KB 0x009FF-0x00200 |
| Peripherals | 16-bit | 0x001FF-0x00100 | 0x001FF-0x00100 | 0x001FF-0x00100 | 0x001FF-0x00100 |
| | 8-bit | 0x000FF-0x00010 | 0x000FF-0x00010 | 0x000FF-0x00010 | 0x000FF-0x00010 |
| | 8-bit SFR | 0x0000F-0x00000 | 0x0000F-0x00000 | 0x0000F-0x00000 | 0x0000F-0x00000 |

Bootstrap Loader (BSL)

The MSP430 BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by a user-defined password. For complete description of the features of the BSL and its implementation, see the *MSP430 Programming Via the Bootstrap Loader (BSL) User's Guide (SLAU319)*.

Table 9. BSL Pin Functions

| BSL FUNCTION | PM, PN PACKAGE PINS | ZQW PACKAGE PINS |
|---------------|---------------------|------------------|
| Data Transmit | 13 - P1.1 | H1 - P1.1 |
| Data Receive | 22 - P2.2 | M3 - P2.2 |

Flash Memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset segment A is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.
- Flash content integrity check with marginal read modes

Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide (SLAU144)*.

DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12 conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode without having to awaken to move data to or from a peripheral.

Oscillator and System Clock

The clock system in the MSP430F241x and MSP430F261x family of devices is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very low-power low-frequency oscillator, an internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 μ s. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

The DCO settings to calibrate the DCO output frequency are stored in the information memory segment A.

Calibration Data Stored in Information Memory Segment A

Calibration data is stored for the DCO and for the ADC12. It is organized in a tag-length-value (TLV) structure.

Table 10. Tags Used by the TLV Structure

| NAME | ADDRESS | VALUE | DESCRIPTION |
|-------------|---------|-------|---|
| TAG_DCO_30 | 0x10F6 | 0x01 | DCO frequency calibration at $V_{CC} = 3$ V and $T_A = 25^\circ\text{C}$ at calibration |
| TAG_ADC12_1 | 0x10DA | 0x08 | ADC12_1 calibration tag |
| TAG_EMPTY | - | 0xFE | Identifier for empty memory areas |

Table 11. Labels Used by the ADC Calibration Structure

| LABEL | CONDITION AT CALIBRATION | SIZE | ADDRESS OFFSET |
|-----------------------|--|------|----------------|
| CAL_ADC_25T85 | INCHx = 0x1010, REF2_5 = 1, $T_A = 85^\circ\text{C}$ | word | 0x000E |
| CAL_ADC_25T30 | INCHx = 0x1010, REF2_5 = 1, $T_A = 30^\circ\text{C}$ | word | 0x000C |
| CAL_ADC_25VREF_FACTOR | REF2_5 = 1, $T_A = 30^\circ\text{C}$ | word | 0x000A |
| CAL_ADC_15T85 | INCHx = 0x1010, REF2_5 = 0, $T_A = 85^\circ\text{C}$ | word | 0x0008 |
| CAL_ADC_15T30 | INCHx = 0x1010, REF2_5 = 0, $T_A = 30^\circ\text{C}$ | word | 0x0006 |
| CAL_ADC_15VREF_FACTOR | REF2_5 = 0, $T_A = 30^\circ\text{C}$ | word | 0x0004 |
| CAL_ADC_OFFSET | External $V_{REF} = 1.5$ V, $f_{ADC12CLK} = 5$ MHz | word | 0x0002 |
| CAL_ADC_GAIN_FACTOR | External $V_{REF} = 1.5$ V, $f_{ADC12CLK} = 5$ MHz | word | 0x0000 |
| CAL_BC1_1MHZ | - | byte | 0x0007 |
| CAL_DCO_1MHZ | - | byte | 0x0006 |
| CAL_BC1_8MHZ | - | byte | 0x0005 |
| CAL_DCO_8MHZ | - | byte | 0x0004 |
| CAL_BC1_12MHZ | - | byte | 0x0003 |
| CAL_DCO_12MHZ | - | byte | 0x0002 |
| CAL_BC1_16MHZ | - | byte | 0x0001 |
| CAL_DCO_16MHZ | - | byte | 0x0000 |

Brownout, Supply Voltage Supervisor (SVS)

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM) (the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must ensure that the default DCO settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

Digital I/O

There are up to eight 8-bit I/O ports implemented—ports P1 through P8:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and port P2.
- Read and write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup or pulldown resistor.
- Ports P7 and P8 can be accessed word-wise.

Watchdog Timer (WDT+)

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs 16x16, 16x8, 8x16, and 8x8 bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

Universal Serial Communication Interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 pin or 4 pin) or I²C, and asynchronous combination protocols such as UART, enhanced UART with automatic baudrate detection (LIN), and IrDA.

The USCI_A module provides support for SPI (3 pin or 4 pin), UART, enhanced UART, and IrDA.

The USCI_B module provides support for SPI (3 pin or 4 pin) and I²C

Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 12. Timer_A3 Signal Connections

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|------------------|-----------|---------------------|-------------------|--------------------|----------------------|--------------------|-----------|
| ZQW | PM, PN | | | | | PM, PN | ZQW |
| G2 - P1.0 | 12 - P1.0 | TACLK | TACLK | Timer | NA | | |
| | | ACLK | ACLK | | | | |
| | | SMCLK | SMCLK | | | | |
| M2 - P2.1 | 21 - P2.1 | TAINCLK | INCLK | | | | |
| H1 - P1.1 | 13 - P1.1 | TA0 | CC10A | CCR0 | TA0 | 13 - P1.1 | H1 - P1.1 |
| M3 - P2.2 | 22 - P2.2 | TA0 | CC10B | | | 17 - P1.5 | K1 - P1.5 |
| | | DV _{SS} | GND | | | 27 - P2.7 | L5 - P2.7 |
| | | DV _{CC} | V _{CC} | | | | |
| H2 - P1.2 | 14 - P1.2 | TA1 | CC11A | CCR1 | TA1 | 14 - P1.2 | H2 - P1.2 |
| | | CAOUT (internal) | CC11B | | | 18 - P1.6 | K2 - P1.6 |
| | | DV _{SS} | GND | | | 23 - P2.3 | L3 - P2.3 |
| | | DV _{CC} | V _{CC} | | | ADC12 (internal) | |
| | | | | | | DAC12_0 (internal) | |
| | | | | DAC12_1 (internal) | | | |
| J1 - P1.3 | 15 - P1.3 | TA2 | CC12A | CCR2 | TA2 | 15 - P1.3 | J1 - P1.3 |
| | | ACLK (internal) | CC12B | | | 19 - P1.7 | L1 - P1.7 |
| | | DV _{SS} | GND | | | 24 - P2.4 | L4 - P2.4 |
| | | DV _{CC} | V _{CC} | | | | |

Timer_B7

Timer_B7 is a 16-bit timer/counter with seven capture/compare registers. Timer_B7 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B7 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 13. Timer_B3, Timer_B7 Signal Connections

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|------------------|-----------|---------------------|-------------------|--------------|----------------------|-------------------|------------|
| ZQW | PM, PN | | | | | PM, PN | ZQW |
| K11 - P4.7 | 43 - P4.7 | TBCLK | TBCLK | Timer | NA | | |
| | | ACLK | ACLK | | | | |
| | | SMCLK | SMCLK | | | | |
| K11 - P4.7 | 43 - P4.7 | TBCLK | INCLK | | | | |
| M9 - P4.0 | 36 - P4.0 | TB0 | CCI0A | CCR0 | TB0 | 36 - P4.0 | M9 - P4.0 |
| M9 - P4.0 | 36 - P4.0 | TB0 | CCI0B | | | ADC12 (internal) | |
| | | DV _{SS} | GND | | | | |
| | | DV _{CC} | V _{CC} | | | | |
| J9 - P4.1 | 37 - P4.1 | TB1 | CCI1A | CCR1 | TB1 | 37 - P4.1 | J9 - P4.1 |
| J9 - P4.1 | 37 - P4.1 | TB1 | CCI1B | | | ADC12 (internal) | |
| | | DV _{SS} | GND | | | | |
| | | DV _{CC} | V _{CC} | | | | |
| M10 - P4.2 | 38 - P4.2 | TB2 | CCI2A | CCR2 | TB2 | 38 - P4.2 | M10 - P4.2 |
| M10 - P4.2 | 38 - P4.2 | TB2 | CCI2B | | | DAC_0 (internal) | |
| | | DV _{SS} | GND | | | DAC_1 (internal) | |
| | | DV _{CC} | V _{CC} | | | | |
| L10 - P4.3 | 39 - P4.3 | TB3 | CCI3A | CCR3 | TB3 | 39 - P4.3 | L10 - P4.3 |
| L10 - P4.3 | 39 - P4.3 | TB3 | CCI3B | | | | |
| | | DV _{SS} | GND | | | | |
| | | DV _{CC} | V _{CC} | | | | |
| M11 - P4.4 | 40 - P4.4 | TB4 | CCI4A | CCR4 | TB4 | 40 - P4.4 | M11 - P4.4 |
| M11 - P4.4 | 40 - P4.4 | TB4 | CCI4B | | | | |
| | | DV _{SS} | GND | | | | |
| | | DV _{CC} | V _{CC} | | | | |
| M12 - P4.5 | 41 - P4.5 | TB5 | CCI5A | CCR5 | TB5 | 41 - P4.5 | M12 - P4.5 |
| M12 - P4.5 | 41 - P4.5 | TB5 | CCI5B | | | | |
| | | DV _{SS} | GND | | | | |
| | | DV _{CC} | V _{CC} | | | | |
| L12 - P4.6 | 42 - P4.6 | TB6 | CCI6A | CCR6 | TB6 | 42 - P4.6 | L12 - P4.6 |
| | | ACLK (internal) | CCI6B | | | | |
| | | DV _{SS} | GND | | | | |
| | | DV _{CC} | V _{CC} | | | | |

Comparator_A+

The primary function of the Comparator_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

ADC12

The ADC12 module supports fast 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator, and a 16-word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

DAC12

The DAC12 module is a 12-bit R-ladder voltage-output digital-to-analog converter (DAC). The DAC12 may be used in 8-bit or 12-bit mode and may be used in conjunction with the DMA controller. When multiple DAC12 modules are present, they may be grouped together for synchronous operation.

Peripheral File Map

Table 14. Peripherals File Map

| MODULE | REGISTER | SHORT FORM | ADDRESS |
|----------------------|-----------------------------------|------------|---------|
| DMA ⁽¹⁾ | DMA channel 2 transfer size | DMA2SZ | 0x01F2 |
| | DMA channel 2 destination address | DMA2DA | 0x01EE |
| | DMA channel 2 source address | DMA2SA | 0x01EA |
| | DMA channel 2 control | DMA2CTL | 0x01E8 |
| | DMA channel 1 transfer size | DMA1SZ | 0x01E6 |
| | DMA channel 1 destination address | DMA1DA | 0x01E2 |
| | DMA channel 1 source address | DMA1SA | 0x01DE |
| | DMA channel 1 control | DMA1CTL | 0x01DC |
| | DMA channel 0 transfer size | DMA0SZ | 0x01DA |
| | DMA channel 0 destination address | DMA0DA | 0x01D6 |
| | DMA channel 0 source address | DMA0SA | 0x01D2 |
| | DMA channel 0 control | DMA0CTL | 0x01D0 |
| | DMA module interrupt vector word | DMAIV | 0x0126 |
| | DMA module control 1 | DMACTL1 | 0x0124 |
| DMA module control 0 | DMACTL0 | 0x0122 | |
| DAC12 ⁽¹⁾ | DAC12_1 data | DAC12_1DAT | 0x01CA |
| | DAC12_1 control | DAC12_1CTL | 0x01C2 |
| | DAC12_0 data | DAC12_0DAT | 0x01C8 |
| | DAC12_0 control | DAC12_0CTL | 0x01C0 |

(1) MSP430F261x devices only

Table 14. Peripherals File Map (continued)

| MODULE | REGISTER | SHORT FORM | ADDRESS |
|------------------------------|--------------------------------|-------------|---------|
| ADC12 | Interrupt vector word register | ADC12IV | 0x01A8 |
| | Interrupt enable register | ADC12IE | 0x01A6 |
| | Interrupt flag register | ADC12IFG | 0x01A4 |
| | Control register 1 | ADC12CTL1 | 0x01A2 |
| | Control register 0 | ADC12CTL0 | 0x01A0 |
| | Conversion memory 15 | ADC12MEM15 | 0x015E |
| | Conversion memory 14 | ADC12MEM14 | 0x015C |
| | Conversion memory 13 | ADC12MEM13 | 0x015A |
| | Conversion memory 12 | ADC12MEM12 | 0x0158 |
| | Conversion memory 11 | ADC12MEM11 | 0x0156 |
| | Conversion memory 10 | ADC12MEM10 | 0x0154 |
| | Conversion memory 9 | ADC12MEM9 | 0x0152 |
| | Conversion memory 8 | ADC12MEM8 | 0x0150 |
| | Conversion memory 7 | ADC12MEM7 | 0x014E |
| | Conversion memory 6 | ADC12MEM6 | 0x014C |
| | Conversion memory 5 | ADC12MEM5 | 0x014A |
| | Conversion memory 4 | ADC12MEM4 | 0x0148 |
| | Conversion memory 3 | ADC12MEM3 | 0x0146 |
| | Conversion memory 2 | ADC12MEM2 | 0x0144 |
| | Conversion memory 1 | ADC12MEM1 | 0x0142 |
| | Conversion memory 0 | ADC12MEM0 | 0x0140 |
| | ADC memory-control register15 | ADC12MCTL15 | 0x008F |
| | ADC memory-control register14 | ADC12MCTL14 | 0x008E |
| | ADC memory-control register13 | ADC12MCTL13 | 0x008D |
| | ADC memory-control register12 | ADC12MCTL12 | 0x008C |
| | ADC memory-control register11 | ADC12MCTL11 | 0x008B |
| | ADC memory-control register10 | ADC12MCTL10 | 0x008A |
| | ADC memory-control register9 | ADC12MCTL9 | 0x0089 |
| | ADC memory-control register8 | ADC12MCTL8 | 0x0088 |
| | ADC memory-control register7 | ADC12MCTL7 | 0x0087 |
| | ADC memory-control register6 | ADC12MCTL6 | 0x0086 |
| | ADC memory-control register5 | ADC12MCTL5 | 0x0085 |
| | ADC memory-control register4 | ADC12MCTL4 | 0x0084 |
| | ADC memory-control register3 | ADC12MCTL3 | 0x0083 |
| ADC memory-control register2 | ADC12MCTL2 | 0x0082 | |
| ADC memory-control register1 | ADC12MCTL1 | 0x0081 | |
| ADC memory-control register0 | ADC12MCTL0 | 0x0080 | |

Table 14. Peripherals File Map (continued)

| MODULE | REGISTER | SHORT FORM | ADDRESS |
|----------------------------|---------------------------------------|----------------------------|---------|
| Timer_B7 | Capture/compare register 6 | TBCCR6 | 0x019E |
| | Capture/compare register 5 | TBCCR5 | 0x019C |
| | Capture/compare register 4 | TBCCR4 | 0x019A |
| | Capture/compare register 3 | TBCCR3 | 0x0198 |
| | Capture/compare register 2 | TBCCR2 | 0x0196 |
| | Capture/compare register 1 | TBCCR1 | 0x0194 |
| | Capture/compare register 0 | TBCCR0 | 0x0192 |
| | Timer_B register | TBR | 0x0190 |
| | Capture/compare control 6 | TBCCTL6 | 0x018E |
| | Capture/compare control 5 | TBCCTL5 | 0x018C |
| | Capture/compare control 4 | TBCCTL4 | 0x018A |
| | Capture/compare control 3 | TBCCTL3 | 0x0188 |
| | Capture/compare control 2 | TBCCTL2 | 0x0186 |
| | Capture/compare control 1 | TBCCTL1 | 0x0184 |
| | Capture/compare control 0 | TBCCTL0 | 0x0182 |
| | Timer_B control | TBCTL | 0x0180 |
| | Timer_B interrupt vector | TBIV | 0x011E |
| | Timer_A3 | Capture/compare register 2 | TACCR2 |
| Capture/compare register 1 | | TACCR1 | 0x0174 |
| Capture/compare register 0 | | TACCR0 | 0x0172 |
| Timer_A register | | TAR | 0x0170 |
| Reserved | | | 0x016E |
| Reserved | | | 0x016C |
| Reserved | | | 0x016A |
| Reserved | | | 0x0168 |
| Capture/compare control 2 | | TACCTL2 | 0x0166 |
| Capture/compare control 1 | | TACCTL1 | 0x0164 |
| Capture/compare control 0 | | TACCTL0 | 0x0162 |
| Timer_A control | | TACTL | 0x0160 |
| Timer_A interrupt vector | | TAIV | 0x012E |
| Hardware Multiplier | | Sum extend | SUMEXT |
| | Result high word | RESHI | 0x013C |
| | Result low word | RESLO | 0x013A |
| | Second operand | OP2 | 0x0138 |
| | Multiply signed +accumulate/operand 1 | MACS | 0x0136 |
| | Multiply+accumulate/operand 1 | MAC | 0x0134 |
| | Multiply signed/operand 1 | MPYS | 0x0132 |
| | Multiply unsigned/operand 1 | MPY | 0x0130 |
| Flash | Flash control 4 | FCTL4 | 0x01BE |
| | Flash control 3 | FCTL3 | 0x012C |
| | Flash control 2 | FCTL2 | 0x012A |
| | Flash control 1 | FCTL1 | 0x0128 |
| Watchdog | Watchdog Timer control | WDTCTL | 0x0120 |

Table 14. Peripherals File Map (continued)

| MODULE | REGISTER | SHORT FORM | ADDRESS |
|-----------------------------|--------------------------------|------------|---------|
| USCI_A0/B0 | USCI_A0 auto baud rate control | UCA0ABCTL | 0x005D |
| | USCI_A0 transmit buffer | UCA0TXBUF | 0x0067 |
| | USCI_A0 receive buffer | UCA0RXBUF | 0x0066 |
| | USCI_A0 status | UCA0STAT | 0x0065 |
| | USCI_A0 modulation control | UCA0MCTL | 0x0064 |
| | USCI_A0 baud rate control 1 | UCA0BR1 | 0x0063 |
| | USCI_A0 baud rate control 0 | UCA0BR0 | 0x0062 |
| | USCI_A0 control 1 | UCA0CTL1 | 0x0061 |
| | USCI_A0 control 0 | UCA0CTL0 | 0x0060 |
| | USCI_A0 IrDA receive control | UCA0IRRCTL | 0x005F |
| | USCI_A0 IrDA transmit control | UCA0IRTCLT | 0x005E |
| | USCI_B0 transmit buffer | UCB0TXBUF | 0x006F |
| | USCI_B0 receive buffer | UCB0RXBUF | 0x006E |
| | USCI_B0 status | UCB0STAT | 0x006D |
| | USCI_B0 I2C Interrupt enable | UCB0CIE | 0x006C |
| | USCI_B0 baud rate control 1 | UCB0BR1 | 0x006B |
| | USCI_B0 baud rate control 0 | UCB0BR0 | 0x006A |
| | USCI_B0 control 1 | UCB0CTL1 | 0x0069 |
| | USCI_B0 control 0 | UCB0CTL0 | 0x0068 |
| | USCI_B0 I2C slave address | UCB0SA | 0x011A |
| USCI_B0 I2C own address | UCB0OA | 0x0118 | |
| USCI_A1/B1 | USCI_A1 auto baud rate control | UCA1ABCTL | 0x00CD |
| | USCI_A1 transmit buffer | UCA1TXBUF | 0x00D7 |
| | USCI_A1 receive buffer | UCA1RXBUF | 0x00D6 |
| | USCI_A1 status | UCA1STAT | 0x00D5 |
| | USCI_A1 modulation control | UCA1MCTL | 0x00D4 |
| | USCI_A1 baud rate control 1 | UCA1BR1 | 0x00D3 |
| | USCI_A1 baud rate control 0 | UCA1BR0 | 0x00D2 |
| | USCI_A1 control 1 | UCA1CTL1 | 0x00D1 |
| | USCI_A1 control 0 | UCA1CTL0 | 0x00D0 |
| | USCI_A1 IrDA receive control | UCA1IRRCTL | 0x00CF |
| | USCI_A1 IrDA transmit control | UCA1IRTCLT | 0x00CE |
| | USCI_B1 transmit buffer | UCB1TXBUF | 0x00DF |
| | USCI_B1 receive buffer | UCB1RXBUF | 0x00DE |
| | USCI_B1 status | UCB1STAT | 0x00DD |
| | USCI_B1 I2C Interrupt enable | UCB1CIE | 0x00DC |
| | USCI_B1 baud rate control 1 | UCB1BR1 | 0x00DB |
| | USCI_B1 baud rate control 0 | UCB1BR0 | 0x00DA |
| | USCI_B1 control 1 | UCB1CTL1 | 0x00D9 |
| | USCI_B1 control 0 | UCB1CTL0 | 0x00D8 |
| | USCI_B1 I2C slave address | UCB1SA | 0x017E |
| USCI_B1 I2C own address | UCB1OA | 0x017C | |
| USCI_A1/B1 interrupt enable | UC1IE | 0x0006 | |
| USCI_A1/B1 interrupt flag | UC1IFG | 0x0007 | |
| Comparator_A+ | Comparator_A port disable | CAPD | 0x005B |
| | Comparator_A control2 | CACTL2 | 0x005A |
| | Comparator_A control1 | CACTL1 | 0x0059 |

Table 14. Peripherals File Map (continued)

| MODULE | REGISTER | SHORT FORM | ADDRESS |
|------------------------|---|------------|---------|
| Basic Clock | Basic clock system control 3 | BCSCTL3 | 0x0053 |
| | Basic clock system control 2 | BCSCTL2 | 0x0058 |
| | Basic clock system control 1 | BCSCTL1 | 0x0057 |
| | DCO clock frequency control | DCOCTL | 0x0056 |
| Brownout, SVS | SVS control register (reset by brownout signal) | SVSCTL | 0x0055 |
| Port PA ⁽²⁾ | Port PA resistor enable | PAREN | 0x0014 |
| | Port PA selection | PASEL | 0x003E |
| | Port PA direction | PADIR | 0x003C |
| | Port PA output | PAOUT | 0x003A |
| | Port PA input | PAIN | 0x0038 |
| Port P8 ⁽²⁾ | Port P8 resistor enable | P8REN | 0x0015 |
| | Port P8 selection | P8SEL | 0x003F |
| | Port P8 direction | P8DIR | 0x003D |
| | Port P8 output | P8OUT | 0x003B |
| | Port P8 input | P8IN | 0x0039 |
| Port P7 ⁽³⁾ | Port P7 resistor enable | P7REN | 0x0014 |
| | Port P7 selection | P7SEL | 0x003E |
| | Port P7 direction | P7DIR | 0x003C |
| | Port P7 output | P7OUT | 0x003A |
| | Port P7 input | P7IN | 0x0038 |
| Port P6 | Port P6 resistor enable | P6REN | 0x0013 |
| | Port P6 selection | P6SEL | 0x0037 |
| | Port P6 direction | P6DIR | 0x0036 |
| | Port P6 output | P6OUT | 0x0035 |
| | Port P6 input | P6IN | 0x0034 |
| Port P5 | Port P5 resistor enable | P5REN | 0x0012 |
| | Port P5 selection | P5SEL | 0x0033 |
| | Port P5 direction | P5DIR | 0x0032 |
| | Port P5 output | P5OUT | 0x0031 |
| | Port P5 input | P5IN | 0x0030 |
| Port P4 | Port P4 selection | P4SEL | 0x001F |
| | Port P4 resistor enable | P4REN | 0x0011 |
| | Port P4 direction | P4DIR | 0x001E |
| | Port P4 output | P4OUT | 0x001D |
| | Port P4 input | P4IN | 0x001C |
| Port P3 | Port P3 resistor enable | P3REN | 0x0010 |
| | Port P3 selection | P3SEL | 0x001B |
| | Port P3 direction | P3DIR | 0x001A |
| | Port P3 output | P3OUT | 0x0019 |
| | Port P3 input | P3IN | 0x0018 |

(2) 80-pin PN and 113-pin ZQW devices only

(3) 80-pin PN and 113-pin ZQW devices only

Table 14. Peripherals File Map (continued)

| MODULE | REGISTER | SHORT FORM | ADDRESS |
|-------------------|-------------------------------|------------|---------|
| Port P2 | Port P2 resistor enable | P2REN | 0x002F |
| | Port P2 selection | P2SEL | 0x002E |
| | Port P2 interrupt enable | P2IE | 0x002D |
| | Port P2 interrupt-edge select | P2IES | 0x002C |
| | Port P2 interrupt flag | P2IFG | 0x002B |
| | Port P2 direction | P2DIR | 0x002A |
| | Port P2 output | P2OUT | 0x0029 |
| | Port P2 input | P2IN | 0x0028 |
| Port P1 | Port P1 resistor enable | P1REN | 0x0027 |
| | Port P1 selection | P1SEL | 0x0026 |
| | Port P1 interrupt enable | P1IE | 0x0025 |
| | Port P1 interrupt-edge select | P1IES | 0x0024 |
| | Port P1 interrupt flag | P1IFG | 0x0023 |
| | Port P1 direction | P1DIR | 0x0022 |
| | Port P1 output | P1OUT | 0x0021 |
| | Port P1 input | P1IN | 0x0020 |
| Special Functions | SFR interrupt flag 2 | IFG2 | 0x0003 |
| | SFR interrupt flag 1 | IFG1 | 0x0002 |
| | SFR interrupt enable 2 | IE2 | 0x0001 |
| | SFR interrupt enable 1 | IE1 | 0x0000 |

Absolute Maximum Ratings⁽¹⁾

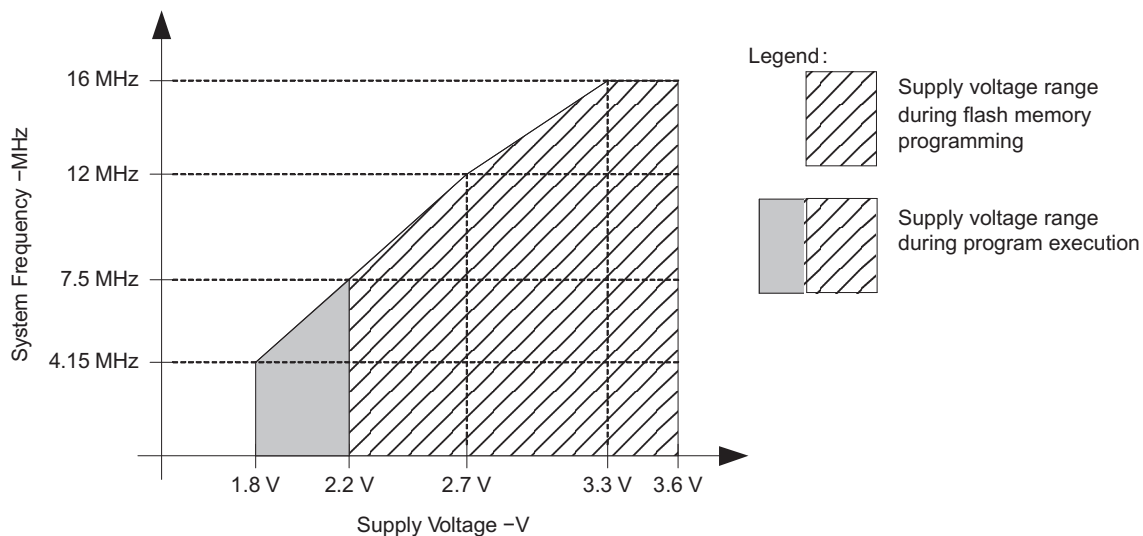
| | | | |
|---|------------------------------------|----------------------------|----------------|
| Voltage applied at V_{CC} to V_{SS} | | -0.3 V to 4.1 V | |
| Voltage applied to any pin ⁽²⁾ | | -0.3 V to $V_{CC} + 0.3$ V | |
| Diode current at any device terminal | | ± 2 mA | |
| T_{stg} | Storage temperature ⁽³⁾ | Unprogrammed device | -55°C to 150°C |
| | | Programmed device | -55°C to 150°C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to V_{SS} . The JTAG fuse-blow voltage, V_{FB} , is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
- (3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Recommended Operating Conditions

| | | MIN | MAX | UNIT | |
|--------------|--|--|-----|------|-----|
| V_{CC} | Supply voltage ($AV_{CC} = DV_{CC} = V_{CC}$ ⁽¹⁾) | During program execution | 1.8 | 3.6 | V |
| | | During flash program/erase | 2.2 | 3.6 | |
| V_{SS} | Supply voltage ($AV_{SS} = DV_{SS} = V_{SS}$) | 0 | 0 | V | |
| T_A | Operating free-air temperature | I version | -40 | 85 | °C |
| | | T version | -40 | 105 | |
| f_{SYSTEM} | Processor frequency (maximum MCLK frequency) ⁽²⁾⁽³⁾ | $V_{CC} = 1.8$ V, Duty cycle = 50% \pm 10% | dc | 4.15 | MHz |
| | | $V_{CC} = 2.7$ V, Duty cycle = 50% \pm 10% | dc | 12 | |
| | | $V_{CC} \geq 3.3$ V, Duty cycle = 50% \pm 10% | dc | 16 | |

- (1) It is recommended to power AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power-up.
- (2) The MSP430 CPU is clocked directly with MCLK. Both the high and low phases of MCLK must not exceed the pulse duration of the specified maximum frequency.
- (3) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.



Note: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Operating Area

Electrical Characteristics

Active Mode Supply Current Into V_{CC} Excluding External Current

 over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾⁽²⁾

| PARAMETER | TEST CONDITIONS | T_A | V_{CC} | MIN | TYP | MAX | UNIT |
|--|---|---------------|----------|-----|-----|---------|------|
| $I_{AM,1MHz}$ Active mode (AM) current (1 MHz) | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 1$ MHz, $f_{ACLK} = 32768$ Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0 | -40°C to 85°C | 2.2 V | 365 | 395 | μ A | |
| | | 105°C | | 375 | 420 | | |
| | | -40°C to 85°C | 3 V | 515 | 560 | | |
| | | 105°C | | 525 | 595 | | |
| $I_{AM,1MHz}$ Active mode (AM) current (1 MHz) | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 1$ MHz, $f_{ACLK} = 32768$ Hz, Program executes in RAM, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0 | -40°C to 85°C | 2.2 V | 330 | 370 | μ A | |
| | | 105°C | | 340 | 390 | | |
| | | -40°C to 85°C | 3 V | 460 | 495 | | |
| | | 105°C | | 470 | 520 | | |
| $I_{AM,4kHz}$ Active mode (AM) current (4 kHz) | $f_{MCLK} = f_{SMCLK} = f_{ACLK} = 32768$ Hz/8 = 4096 Hz, $f_{DCO} = 0$ Hz, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCG0 = 1, SCG1 = 0, OSCOFF = 0 | -40°C to 85°C | 2.2 V | 2.1 | 9 | μ A | |
| | | 105°C | 2.2 V | 15 | 31 | | |
| | | -40°C to 85°C | 3 V | 3 | 11 | | |
| | | 105°C | 3 V | 19 | 32 | | |
| $I_{AM,100kHz}$ Active mode (AM) current (100 kHz) | $f_{MCLK} = f_{SMCLK} = f_{DCO(0,0)} \approx 100$ kHz, $f_{ACLK} = 0$ Hz, Program executes in flash, RSELx = 0, DCOx = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 1 | -40°C to 85°C | 2.2 V | 67 | 86 | μ A | |
| | | 105°C | 2.2 V | 80 | 99 | | |
| | | -40°C to 85°C | 3 V | 84 | 107 | | |
| | | 105°C | 3 V | 99 | 128 | | |

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

Typical Characteristics - Active Mode Supply Current (Into V_{CC})

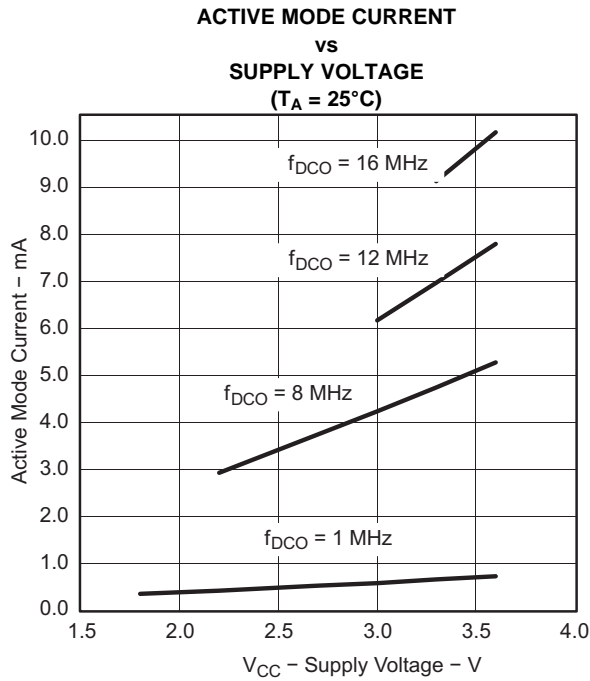


Figure 2.

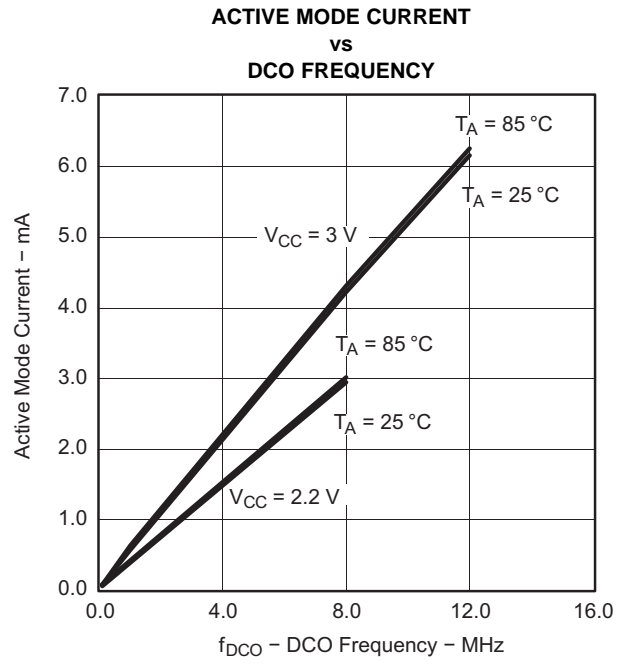


Figure 3.

Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

 over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)^{(1) (2)}

| PARAMETER | TEST CONDITIONS | T_A | V_{CC} | MIN | TYP | MAX | UNIT |
|-------------------|--|---------------|----------|------|------|---------|------|
| $I_{LPM0,1MHz}$ | Low-power mode 0 (LPM0) current ⁽³⁾ $f_{MCLK} = 0$ MHz, $f_{SMCLK} = f_{DCO} = 1$ MHz, $f_{ACLK} = 32,768$ Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 | -40°C to 85°C | 2.2 V | 68 | 63 | μ A | |
| | | 105°C | | 83 | 98 | | |
| | | -40°C to 85°C | 3 V | 87 | 105 | | |
| | | 105°C | | 100 | 125 | | |
| $I_{LPM0,100kHz}$ | Low-power mode 0 (LPM0) current ⁽³⁾ $f_{MCLK} = 0$ MHz, $f_{SMCLK} = f_{DCO(0,0)} \approx 100$ kHz, $f_{ACLK} = 0$ Hz, RSELX = 0, DCOx = 0, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 1 | -40°C to 85°C | 2.2 V | 37 | 49 | μ A | |
| | | 105°C | | 50 | 62 | | |
| | | -40°C to 85°C | 3 V | 40 | 55 | | |
| | | 105°C | | 57 | 73 | | |
| I_{LPM2} | Low-power mode 2 (LPM2) current ⁽⁴⁾ $f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{DCO} = 1$ MHz, $f_{ACLK} = 32,768$ Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 | -40°C to 85°C | 2.2 V | 23 | 33 | μ A | |
| | | 105°C | | 35 | 46 | | |
| | | -40°C to 85°C | 3 V | 25 | 36 | | |
| | | 105°C | | 40 | 55 | | |
| $I_{LPM3,LFXT1}$ | Low-power mode 3 (LPM3) current ⁽³⁾ $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{ACLK} = 32,768$ Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 | -40°C | 2.2 V | 0.8 | 1.2 | μ A | |
| | | 25°C | | 1 | 1.3 | | |
| | | 85°C | | 4.6 | 7 | | |
| | | 105°C | | 14 | 24 | | |
| | | -40°C | 3 V | 0.9 | 1.3 | | |
| | | 25°C | | 1.1 | 1.5 | | |
| | | 85°C | | 5.5 | 8 | | |
| | | 105°C | | 17 | 30 | | |
| $I_{LPM3,VLO}$ | Low-power mode 3 (LPM3) current ⁽⁴⁾ $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 | -40°C | 2.2 V | 0.4 | 1 | μ A | |
| | | 25°C | | 0.5 | 1 | | |
| | | 85°C | | 4.3 | 6.5 | | |
| | | 105°C | | 14 | 24 | | |
| | | -40°C | 3 V | 0.6 | 1.2 | | |
| | | 25°C | | 0.6 | 1.2 | | |
| | | 85°C | | 5 | 7.5 | | |
| | | 105°C | | 16.5 | 29.5 | | |
| I_{LPM4} | Low-power mode 4 (LPM4) current ⁽⁵⁾ $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{ACLK} = 0$ Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 | -40°C | 2.2 V | 0.1 | 0.5 | μ A | |
| | | 25°C | | 0.1 | 0.5 | | |
| | | 85°C | | 4 | 6 | | |
| | | 105°C | | 13 | 23 | | |
| | | -40°C | 3 V | 0.2 | 0.5 | | |
| | | 25°C | | 0.2 | 0.5 | | |
| | | 85°C | | 4.7 | 7 | | |
| | | 105°C | | 14 | 24 | | |

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF.

(3) Current for brownout and WDT clocked by SMCLK included.

(4) Current for brownout and WDT clocked by ACLK included.

(5) Current for brownout included.

Typical Characteristics - LPM4 Current

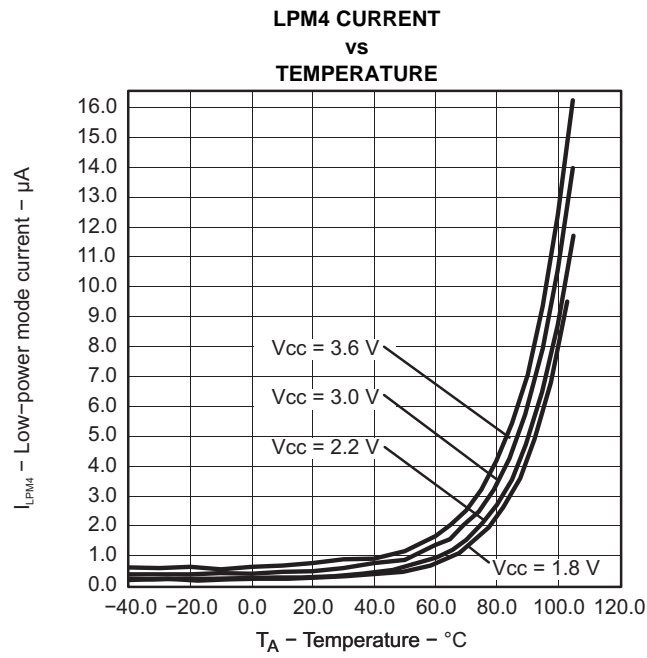


Figure 4.

Schmitt-Trigger Inputs (Ports P1 Through P8, $\overline{\text{RST/NMI}}$, JTAG, XIN, and XT2IN)⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------|---|--|-----------------|----------------------|------|----------------------|------|
| V _{IT+} | Positive-going input threshold voltage | | | 0.45 V _{CC} | | 0.75 V _{CC} | V |
| | | | 2.2 V | 1.00 | 1.65 | | |
| | | | 3 V | 1.35 | 2.25 | | |
| V _{IT-} | Negative-going input threshold voltage | | | 0.25 V _{CC} | | 0.55 V _{CC} | V |
| | | | 2.2 V | 0.55 | 1.20 | | |
| | | | 3 V | 0.75 | 1.65 | | |
| V _{hys} | Input voltage hysteresis (V _{IT+} - V _{IT-}) | | 2.2 V | 0.2 | | 1 | V |
| | | | 3 V | 0.3 | | 1 | |
| R _{Pull} | Pullup/pulldown resistor | For pullup: V _{IN} = V _{SS} , For pulldown: V _{IN} = V _{CC} | | 20 | 35 | 50 | kΩ |
| C _I | Input capacitance | V _{IN} = V _{SS} or V _{CC} | | | 5 | | pF |

(1) XIN and XT2IN in bypass mode only

Inputs (Ports P1 and P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|--------------------|---|-----------------|-----|-----|------|
| t _(int) | External interrupt timing Port P1, P2: P1.x to P2.x, External trigger pulse width to set interrupt flag ⁽¹⁾ | 2.2 V, 3 V | 20 | | ns |

(1) An external signal sets the interrupt flag every time the minimum interrupt pulse width t_(int) is met. It may be set even with trigger signals shorter than t_(int).

Leakage Current (Ports P1 Through P8)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------------|-----------------|-----------------|-----|-----|------|
| I _{lk(Px.y)} | (1) (2) | 2.2 V, 3 V | | ±50 | nA |

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

Standard Inputs ($\overline{\text{RST/NMI}}$)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------|--------------------------|-----------------|---------------------|-----------------------|------|
| V _{IL} | Low-level input voltage | 2.2 V, 3 V | V _{SS} | V _{SS} + 0.6 | V |
| V _{IH} | High-level input voltage | 2.2 V, 3 V | 0.8 V _{CC} | V _{CC} | V |

Outputs (Ports P1 Through P8)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---|---|-----------------|------------------------|------------------------|-----------------|------|
| V _{OH} High-level output voltage | I _(OHmax) = -1.5 mA ⁽¹⁾ | 2.2 V | V _{CC} - 0.25 | | V _{CC} | V |
| | I _(OHmax) = -6 mA ⁽²⁾ | 2.2 V | V _{CC} - 0.6 | | V _{CC} | |
| | I _(OHmax) = -1.5 mA ⁽¹⁾ | 3 V | V _{CC} - 0.25 | | V _{CC} | |
| | I _(OHmax) = -6 mA ⁽²⁾ | 3 V | V _{CC} - 0.6 | | V _{CC} | |
| V _{OL} Low-level output voltage | I _(OLmax) = 1.5 mA ⁽¹⁾ | 2.2 V | V _{SS} | V _{SS} + 0.25 | | V |
| | I _(OLmax) = 6 mA ⁽²⁾ | 2.2 V | V _{SS} | V _{SS} + 0.6 | | |
| | I _(OLmax) = 1.5 mA ⁽¹⁾ | 3 V | V _{SS} | V _{SS} + 0.25 | | |
| | I _(OLmax) = 6 mA ⁽²⁾ | 3 V | V _{SS} | V _{SS} + 0.6 | | |

- (1) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±12 mA to hold the maximum voltage drop specified.
- (2) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

Output Frequency (Ports P1 Through P8)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---|--|-----------------|-------------|-----|-------------|------|
| f _{Px,y} Port output frequency (with load) | P1.4/SMCLK, C _L = 20 pF, R _L = 1 kΩ ⁽¹⁾ (2) | 2.2 V | dc | | 10 | MHz |
| | | 3 V | dc | | 12 | |
| f _{Port*CLK} Clock output frequency | P2.0/ACLK/CA2, P1.4/SMCLK, C _L = 20 pF ⁽²⁾ | 2.2 V | dc | | 12 | MHz |
| | | 3 V | dc | | 16 | |
| t _(Xdc) Duty cycle of output frequency | P5.6/ACLK, C _L = 20 pF, LF mode | | 30 | 50 | 70 | % |
| | P5.6/ACLK, C _L = 20 pF, XT1 mode | | 40 | 50 | 60 | |
| | P5.4/MCLK, C _L = 20 pF, XT1 mode | | 40 | | 60 | |
| | P5.4/MCLK, C _L = 20 pF, DCO | | 50% - 15 ns | | 50% + 15 ns | |
| | P1.4/SMCLK, C _L = 20 pF, XT2 mode | | 40 | | 60 | |
| | P1.4/SMCLK, C _L = 20 pF, DCO | | 50% - 15 ns | | 50% + 15 ns | |

- (1) A resistive divider with two 0.5-kΩ resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
- (2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics - Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

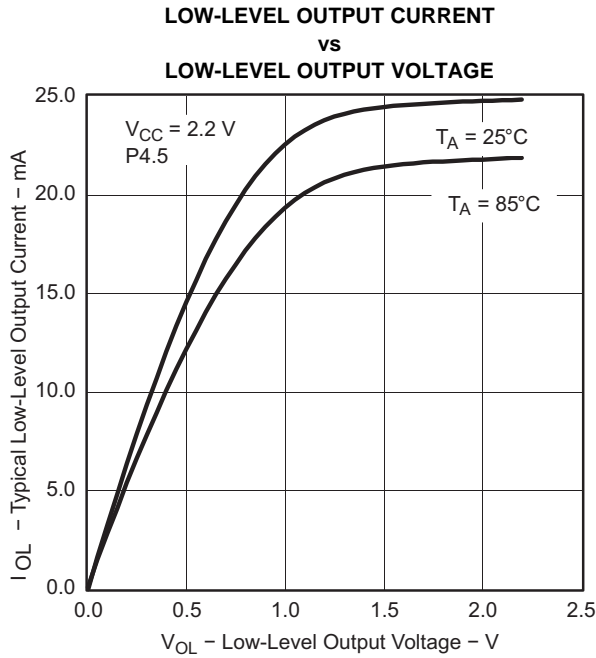


Figure 5.

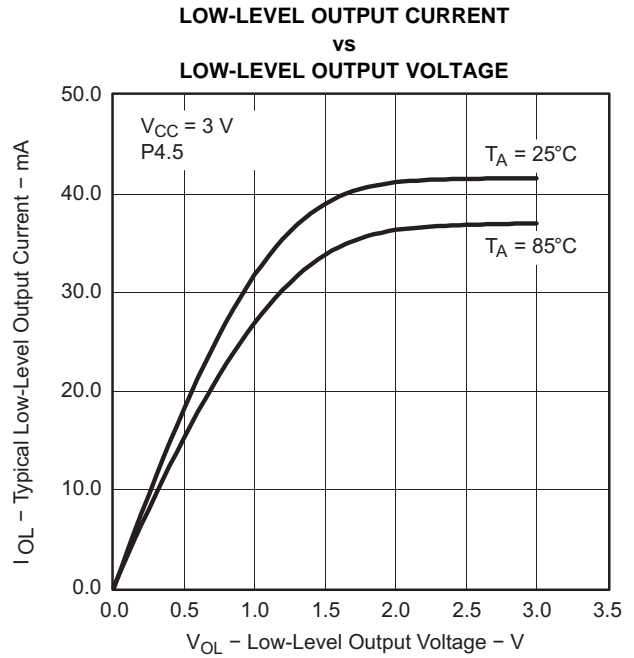


Figure 6.

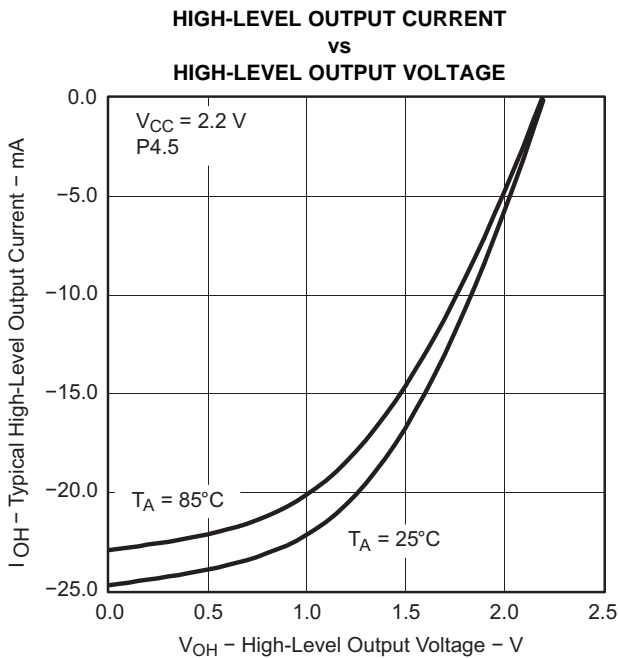


Figure 7.

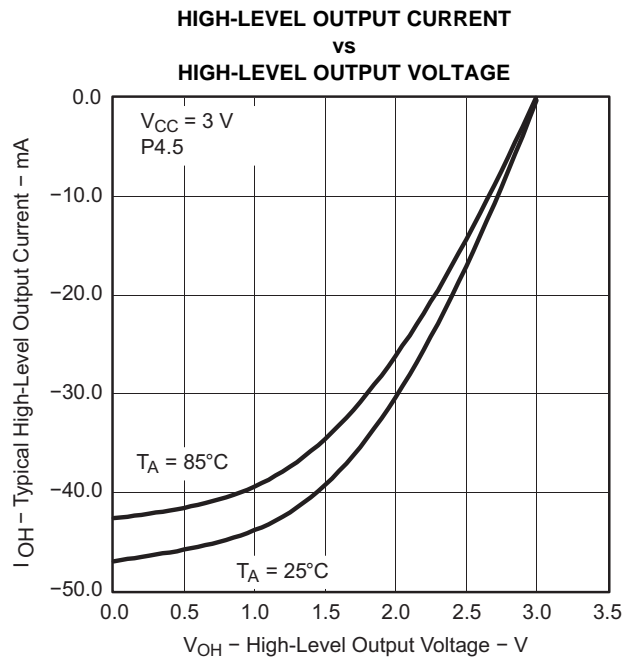


Figure 8.

POR and Brownout Reset (BOR)⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------|--|------------------------------|-----------------|-----|-------------------------------|------|------|
| V _{CC(start)} | See Figure 9 | dV _{CC} /dt ≤ 3 V/s | | | 0.7 × V _(B_IT-) | | V |
| V _(B_IT-) | See Figure 9 through Figure 11 | dV _{CC} /dt ≤ 3 V/s | | | | 1.71 | V |
| V _{hys(B_IT-)} | See Figure 9 | dV _{CC} /dt ≤ 3 V/s | | 70 | 130 | 210 | mV |
| t _{d(BOR)} | See Figure 9 | | | | | 2000 | μs |
| t _(reset) | Pulse length needed at $\overline{\text{RST}}/\text{NMI}$ pin to accepted reset internally | | 2.2 V, 3 V | 2 | | | μs |

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level V_(B_IT-) + V_{hys(B_IT-)} is ≤ 1.8 V.

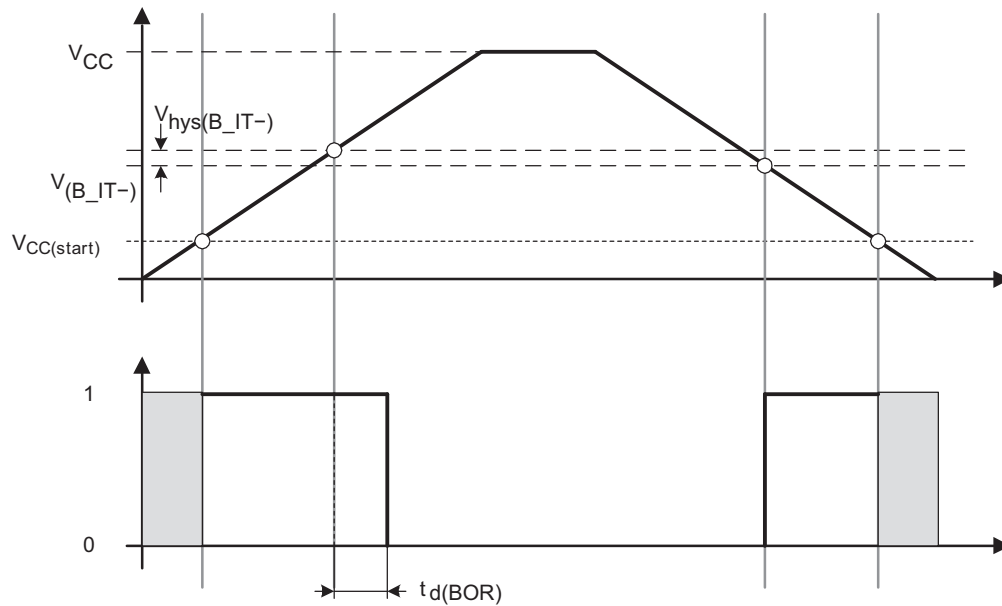


Figure 9. POR and BOR vs Supply Voltage

Typical Characteristics - POR and BOR

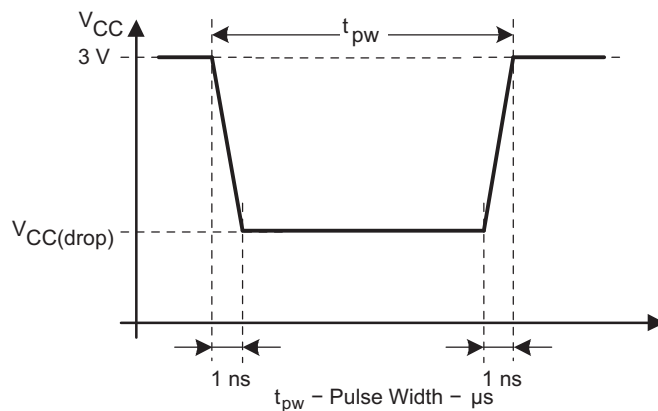
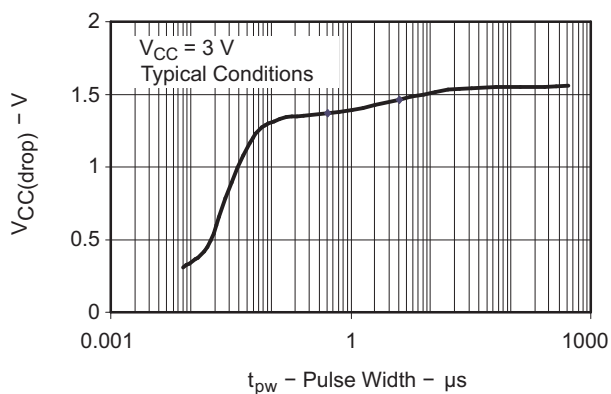


Figure 10. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR for BOR Signal

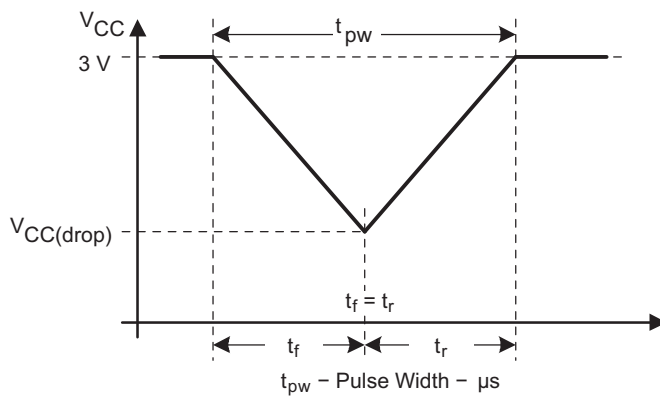
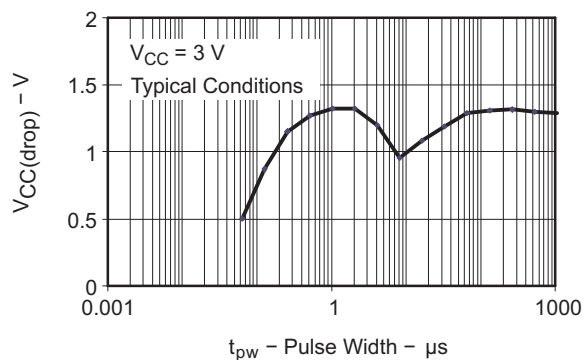


Figure 11. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR or BOR Signal

Supply Voltage Supervisor (SVS), Supply Voltage Monitor (SVM)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|-----------------------------------|--|--|--------------------------------------|--------------------|--------------------------------------|----|
| $t_{(SVSR)}$ | $dV_{CC}/dt > 30 \text{ V/ms}$ (see Figure 12) | 5 | | 150 | μs | |
| | $dV_{CC}/dt \leq 30 \text{ V/ms}$ | | | 2000 | | |
| $t_{d(SV\text{Son})}$ | SVSon, switch from VLD = 0 to VLD \neq 0, $V_{CC} = 3 \text{ V}$ | | 150 | 300 | μs | |
| t_{settle} | VLD \neq 0 ⁽¹⁾ | | | 12 | μs | |
| $V_{(SV\text{Sstart})}$ | VLD \neq 0, $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 12) | | 1.55 | 1.7 | V | |
| $V_{\text{hys}(SV\text{S_IT-})}$ | $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 12) | VLD = 1 | 70 | 120 | 155 | mV |
| | | VLD = 2 to 14 | $0.004 \times V_{(SV\text{S_IT-})}$ | | $0.016 \times V_{(SV\text{S_IT-})}$ | V |
| | $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 12), external voltage applied on A7 | VLD = 15 | 4.4 | | 20 | mV |
| $V_{(SV\text{S_IT-})}$ | $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 12 and Figure 13) | VLD = 1 | 1.8 | 1.9 | 2.05 | V |
| | | VLD = 2 | 1.94 | 2.1 | 2.25 | |
| | | VLD = 3 | 2.05 | 2.2 | 2.37 | |
| | | VLD = 4 | 2.14 | 2.3 | 2.48 | |
| | | VLD = 5 | 2.24 | 2.4 | 2.60 | |
| | | VLD = 6 | 2.33 | 2.5 | 2.71 | |
| | | VLD = 7 | 2.46 | 2.65 | 2.86 | |
| | | VLD = 8 | 2.58 | 2.8 | 3 | |
| | | VLD = 9 | 2.69 | 2.9 | 3.13 | |
| | | VLD = 10 | 2.83 | 3.05 | 3.29 | |
| | | VLD = 11 | 2.94 | 3.2 | 3.42 | |
| | | VLD = 12 | 3.11 | 3.35 | 3.61 ⁽²⁾ | |
| | | VLD = 13 | 3.24 | 3.5 | 3.76 ⁽²⁾ | |
| | | VLD = 14 | 3.43 | 3.7 ⁽²⁾ | 3.99 ⁽²⁾ | |
| | | $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 12 and Figure 13), external voltage applied on A7 | VLD = 15 | 1.1 | 1.2 | |
| $I_{CC(SVS)}$ ⁽³⁾ | VLD \neq 0, $V_{CC} = 2.2 \text{ V}, 3 \text{ V}$ | | 10 | 15 | μA | |

- (1) t_{settle} is the settling time that the comparator output needs to have a stable level after VLD is switched from VLD \neq 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be $>50 \text{ mV}$.
- (2) The recommended operating voltage range is limited to 3.6 V.
- (3) The current consumption of the SVS module is not included in the I_{CC} current consumption data.

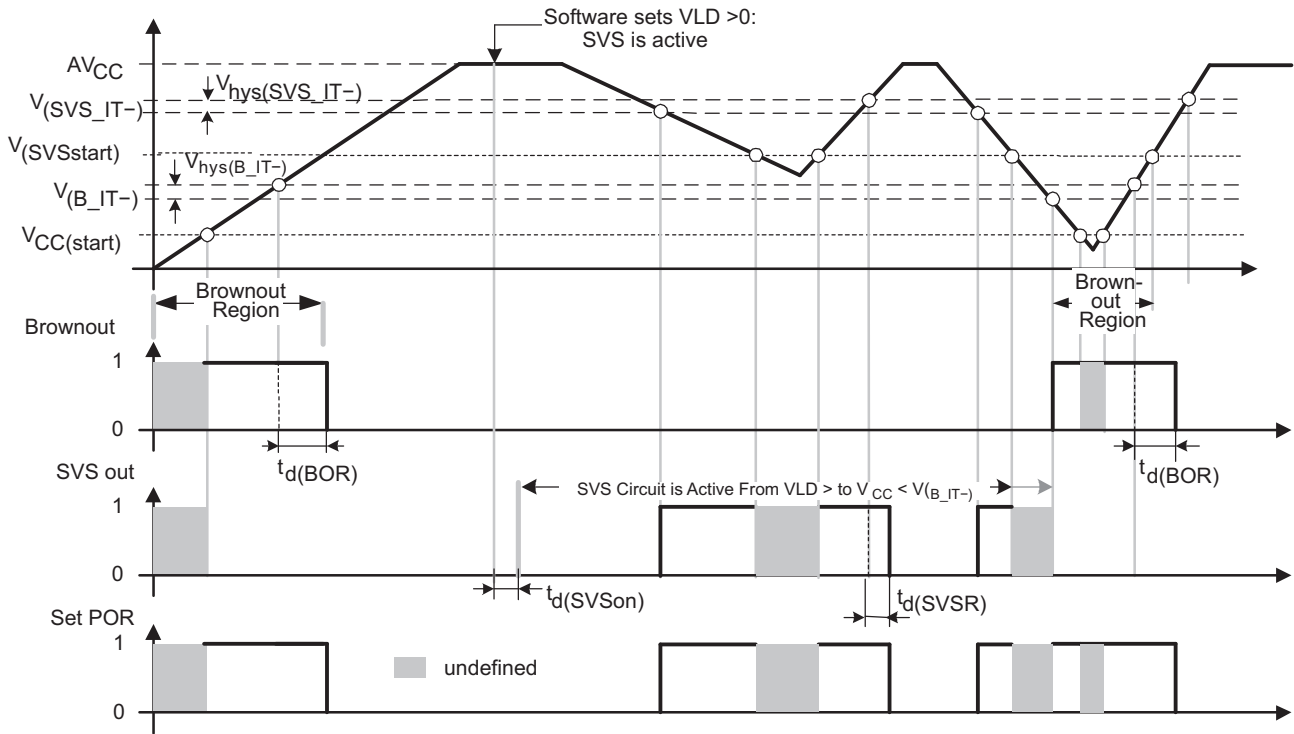


Figure 12. SVS Reset (SVSR) vs Supply Voltage

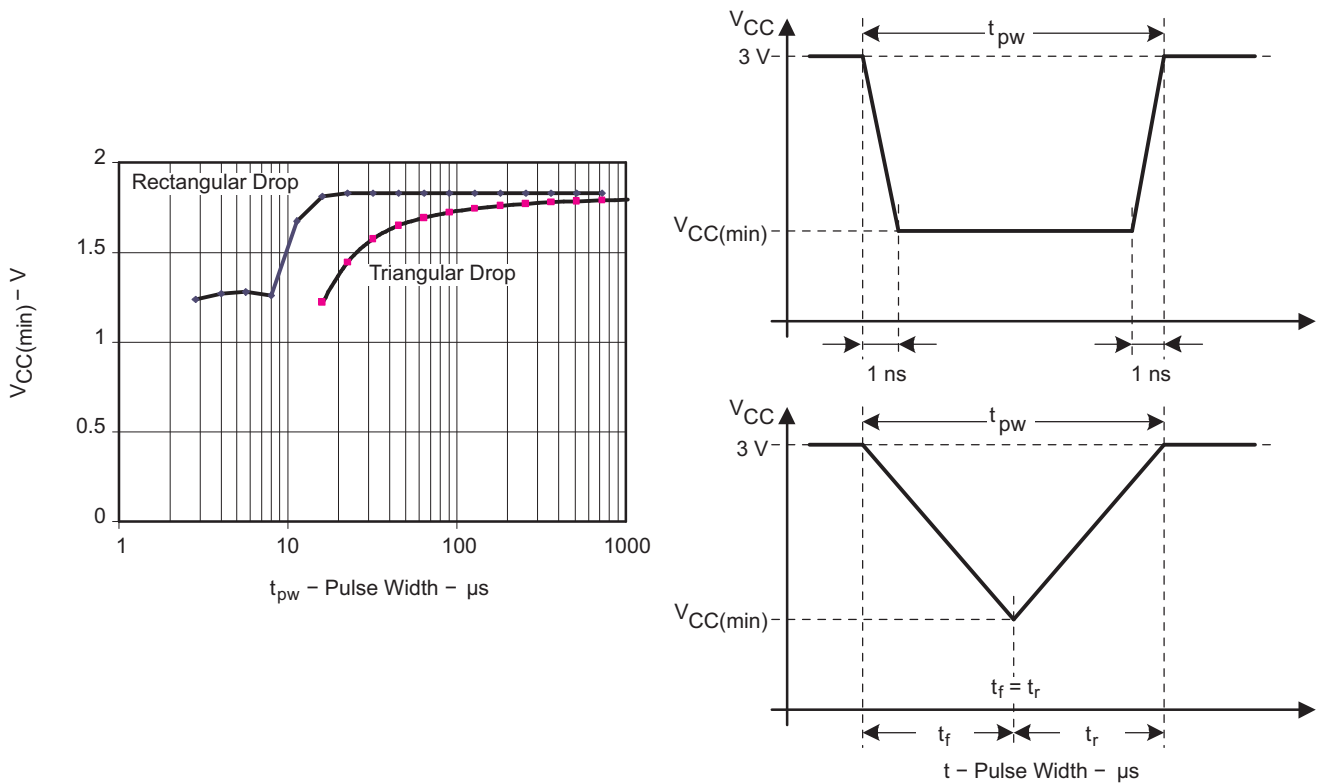


Figure 13. $V_{CC(min)}$: Square Voltage Drop and Triangle Voltage Drop to Generate an SVS Signal (VLD = 1)

Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often f_{DCO(RSEL,DCO+1)} is used within the period of 32 DCOCLK cycles. The frequency f_{DCO(RSEL,DCO)} is used for the remaining cycles. The frequency is an average equal to:

$$f_{\text{average}} = \frac{32 \times f_{\text{DCO(RSEL,DCO)}} \times f_{\text{DCO(RSEL,DCO+1)}}}{\text{MOD} \times f_{\text{DCO(RSEL,DCO)}} + (32 - \text{MOD}) \times f_{\text{DCO(RSEL,DCO+1)}}}$$

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|--|--|-----------------|------|------|------|-------|
| V _{CC} | Supply voltage | RSELx < 14 | | 1.8 | | 3.6 | V |
| | | RSELx = 14 | | 2.2 | | 3.6 | |
| | | RSELx = 15 | | 3.0 | | 3.6 | |
| f _{DCO(0,0)} | DCO frequency (0, 0) | RSELx = 0, DCOx = 0, MODx = 0 | 2.2 V, 3 V | 0.06 | | 0.14 | MHz |
| f _{DCO(0,3)} | DCO frequency (0, 3) | RSELx = 0, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 0.07 | | 0.17 | MHz |
| f _{DCO(1,3)} | DCO frequency (1, 3) | RSELx = 1, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 0.10 | | 0.20 | MHz |
| f _{DCO(2,3)} | DCO frequency (2, 3) | RSELx = 2, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 0.14 | | 0.28 | MHz |
| f _{DCO(3,3)} | DCO frequency (3, 3) | RSELx = 3, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 0.20 | | 0.40 | MHz |
| f _{DCO(4,3)} | DCO frequency (4, 3) | RSELx = 4, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 0.28 | | 0.54 | MHz |
| f _{DCO(5,3)} | DCO frequency (5, 3) | RSELx = 5, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 0.39 | | 0.77 | MHz |
| f _{DCO(6,3)} | DCO frequency (6, 3) | RSELx = 6, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 0.54 | | 1.06 | MHz |
| f _{DCO(7,3)} | DCO frequency (7, 3) | RSELx = 7, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 0.80 | | 1.50 | MHz |
| f _{DCO(8,3)} | DCO frequency (8, 3) | RSELx = 8, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 1.10 | | 2.10 | MHz |
| f _{DCO(9,3)} | DCO frequency (9, 3) | RSELx = 9, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 1.60 | | 3.00 | MHz |
| f _{DCO(10,3)} | DCO frequency (10, 3) | RSELx = 10, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 2.50 | | 4.30 | MHz |
| f _{DCO(11,3)} | DCO frequency (11, 3) | RSELx = 11, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 3.00 | | 5.50 | MHz |
| f _{DCO(12,3)} | DCO frequency (12, 3) | RSELx = 12, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 4.30 | | 7.30 | MHz |
| f _{DCO(13,3)} | DCO frequency (13, 3) | RSELx = 13, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 6.00 | | 9.60 | MHz |
| f _{DCO(14,3)} | DCO frequency (14, 3) | RSELx = 14, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 8.60 | | 13.9 | MHz |
| f _{DCO(15,3)} | DCO frequency (15, 3) | RSELx = 15, DCOx = 3, MODx = 0 | 3 V | 12.0 | | 18.5 | MHz |
| f _{DCO(15,7)} | DCO frequency (15, 7) | RSELx = 15, DCOx = 7, MODx = 0 | 3 V | 16.0 | | 26.0 | MHz |
| S _{RSEL} | Frequency step between range RSEL and RSEL+1 | S _{RSEL} = f _{DCO(RSEL+1,DCO)} /f _{DCO(RSEL,DCO)} | 2.2 V, 3 V | | | 1.55 | ratio |
| S _{DCO} | Frequency step between tap DCO and DCO+1 | S _{DCO} = f _{DCO(RSEL,DCO+1)} /f _{DCO(RSEL,DCO)} | 2.2 V, 3 V | 1.05 | 1.08 | 1.12 | ratio |
| | Duty cycle | Measured at P1.4/SMCLK | 2.2 V, 3 V | 40 | 50 | 60 | % |

Calibrated DCO Frequencies - Tolerance at Calibration

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T _A | V _{CC} | MIN | TYP | MAX | UNIT |
|--|--|----------------|-----------------|-------|------|-------|------|
| Frequency tolerance at calibration | | 25°C | 3 V | -1 | ±0.2 | +1 | % |
| f _{CAL(1MHz)} 1-MHz calibration value | BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms | 25°C | 3 V | 0.990 | 1 | 1.010 | MHz |
| f _{CAL(8MHz)} 8-MHz calibration value | BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms | 25°C | 3 V | 7.920 | 8 | 8.080 | MHz |
| f _{CAL(12MHz)} 12-MHz calibration value | BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms | 25°C | 3 V | 11.88 | 12 | 12.12 | MHz |
| f _{CAL(16MHz)} 16-MHz calibration value | BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms | 25°C | 3 V | 15.84 | 16 | 16.16 | MHz |

Calibrated DCO Frequencies - Tolerance Over Temperature 0°C to 85°C

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T _A | V _{CC} | MIN | TYP | MAX | UNIT |
|--|--|----------------|-----------------|-------|------|-------|------|
| 1-MHz tolerance over temperature | | 0°C to 85°C | 3 V | -2.5 | ±0.5 | +2.5 | % |
| 8-MHz tolerance over temperature | | 0°C to 85°C | 3 V | -2.5 | ±1.0 | +2.5 | % |
| 12-MHz tolerance over temperature | | 0°C to 85°C | 3 V | -2.5 | ±1.0 | +2.5 | % |
| 16-MHz tolerance over temperature | | 0°C to 85°C | 3 V | -3 | ±2.0 | +3 | % |
| f _{CAL(1MHz)} 1-MHz calibration value | BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms | 0°C to 85°C | 2.2 V | 0.970 | 1 | 1.030 | MHz |
| | | | 3 V | 0.975 | 1 | 1.025 | |
| | | | 3.6 V | 0.970 | 1 | 1.030 | |
| f _{CAL(8MHz)} 8-MHz calibration value | BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms | 0°C to 85°C | 2.2 V | 7.760 | 8 | 8.40 | MHz |
| | | | 3 V | 7.800 | 8 | 8.20 | |
| | | | 3.6 V | 7.600 | 8 | 8.24 | |
| f _{CAL(12MHz)} 12-MHz calibration value | BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms | 0°C to 85°C | 2.2 V | 11.64 | 12 | 12.36 | MHz |
| | | | 3 V | 11.64 | 12 | 12.36 | |
| | | | 3.6 V | 11.64 | 12 | 12.36 | |
| f _{CAL(16MHz)} 16-MHz calibration value | BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms | 0°C to 85°C | 3 V | 15.52 | 16 | 16.48 | MHz |
| | | | 3.6 V | 15.00 | 16 | 16.48 | |

Calibrated DCO Frequencies - Tolerance Over Supply Voltage V_{CC}

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T_A | V_{CC} | MIN | TYP | MAX | UNIT |
|---|--|-------|----------------|-------|-----|-------|------|
| 1-MHz tolerance over V_{CC} | | 25°C | 1.8 V to 3.6 V | -3 | ±2 | +3 | % |
| 8-MHz tolerance over V_{CC} | | 25°C | 1.8 V to 3.6 V | -3 | ±2 | +3 | % |
| 12-MHz tolerance over V_{CC} | | 25°C | 2.2 V to 3.6 V | -3 | ±2 | +3 | % |
| 16-MHz tolerance over V_{CC} | | 25°C | 3 V to 3.6 V | -6 | ±2 | +3 | % |
| $f_{CAL(1MHz)}$ 1-MHz calibration value | BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms | 25°C | 1.8 V to 3.6 V | 0.97 | 1 | 1.03 | MHz |
| $f_{CAL(8MHz)}$ 8-MHz calibration value | BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms | 25°C | 1.8 V to 3.6 V | 7.76 | 8 | 8.24 | MHz |
| $f_{CAL(12MHz)}$ 12-MHz calibration value | BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms | 25°C | 2.2 V to 3.6 V | 11.64 | 12 | 12.36 | MHz |
| $f_{CAL(16MHz)}$ 16-MHz calibration value | BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms | 25°C | 3 V to 3.6 V | 15 | 16 | 16.48 | MHz |

Calibrated DCO Frequencies - Overall Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T_A | V_{CC} | MIN | TYP | MAX | UNIT |
|---|--|----------------|----------------|------|-----|------|------|
| 1-MHz tolerance overall | | -40°C to 105°C | 1.8 V to 3.6 V | -5 | ±2 | +5 | % |
| 8-MHz tolerance overall | | -40°C to 105°C | 1.8 V to 3.6 V | -5 | ±2 | +5 | % |
| 12-MHz tolerance overall | | -40°C to 105°C | 2.2 V to 3.6 V | -5 | ±2 | +5 | % |
| 16-MHz tolerance overall | | -40°C to 105°C | 3 V to 3.6 V | -6 | ±3 | +6 | % |
| $f_{CAL(1MHz)}$ 1-MHz calibration value | BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms | -40°C to 105°C | 1.8 V to 3.6 V | 0.95 | 1 | 1.05 | MHz |
| $f_{CAL(8MHz)}$ 8-MHz calibration value | BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms | -40°C to 105°C | 1.8 V to 3.6 V | 7.6 | 8 | 8.4 | MHz |
| $f_{CAL(12MHz)}$ 12-MHz calibration value | BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms | -40°C to 105°C | 2.2 V to 3.6 V | 11.4 | 12 | 12.6 | MHz |
| $f_{CAL(16MHz)}$ 16-MHz calibration value | BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms | -40°C to 105°C | 3 V to 3.6 V | 15 | 16 | 17 | MHz |

Typical Characteristics - Calibrated DCO Frequency

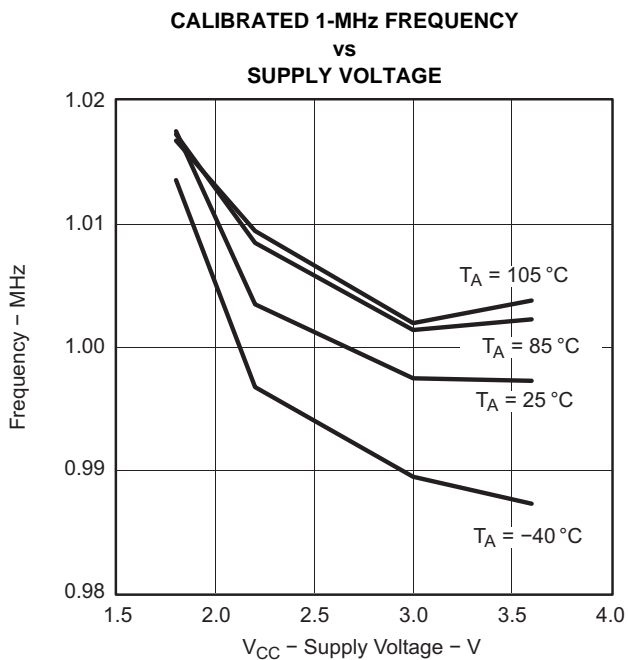


Figure 14.

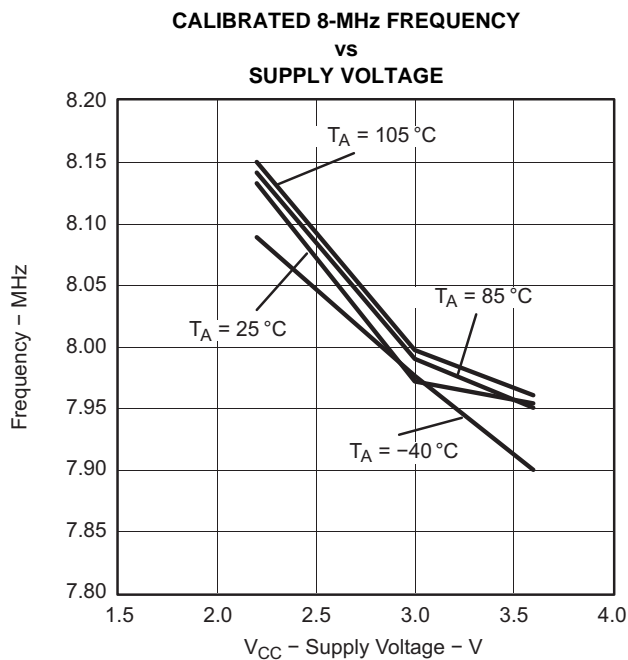


Figure 15.

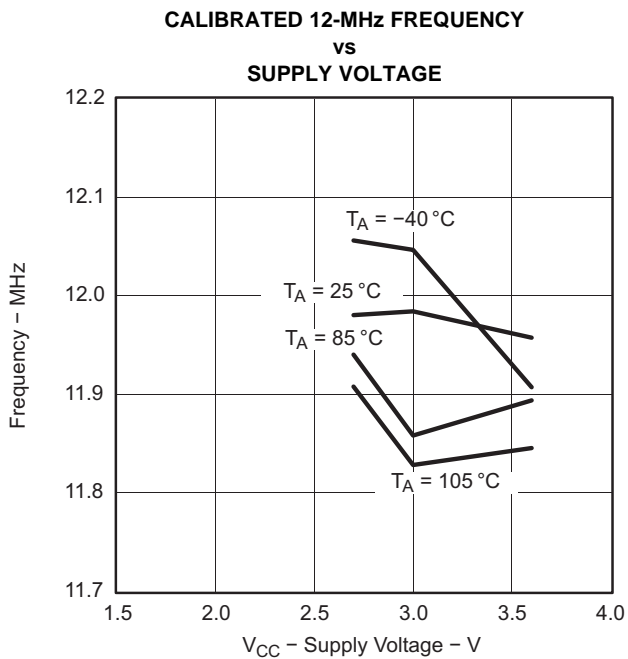


Figure 16.

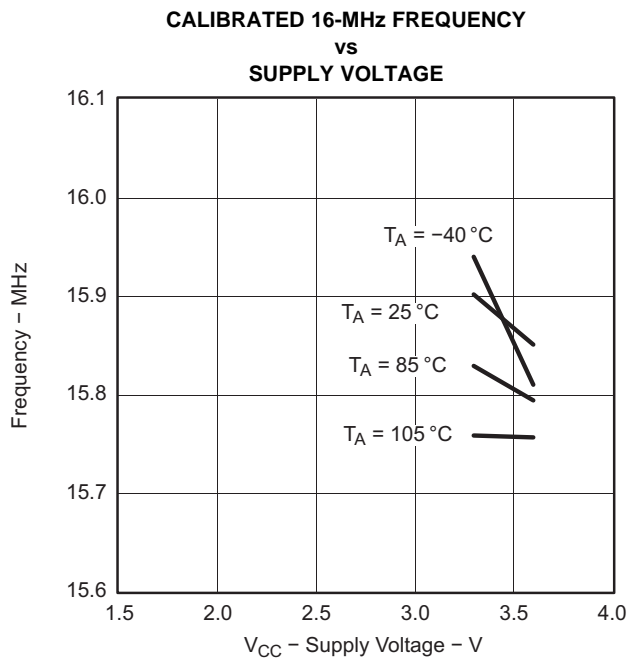


Figure 17.

Wake-Up From Lower-Power Modes (LPM3, LPM4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|--|-----------------|-----|--|-----|------|
| t _{DCO,LPM3/4} DCO clock wake-up time from LPM3 or LPM4 ⁽¹⁾ | BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ | 2.2 V, 3 V | | | 2 | μs |
| | BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ | | | 1.5 | | |
| | BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ | | | 1 | | |
| | BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ | 3 V | | 1 | | |
| t _{CPU,LPM3/4} CPU wake-up time from LPM3 or LPM4 ⁽²⁾ | | | | 1 / f _{MCLK} + t _{Clock,LPM3/4} | | |

- (1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
- (2) Parameter applicable only if DCOCLK is used for MCLK.

Typical Characteristics - DCO Clock Wake-Up Time From LPM3 or LPM4

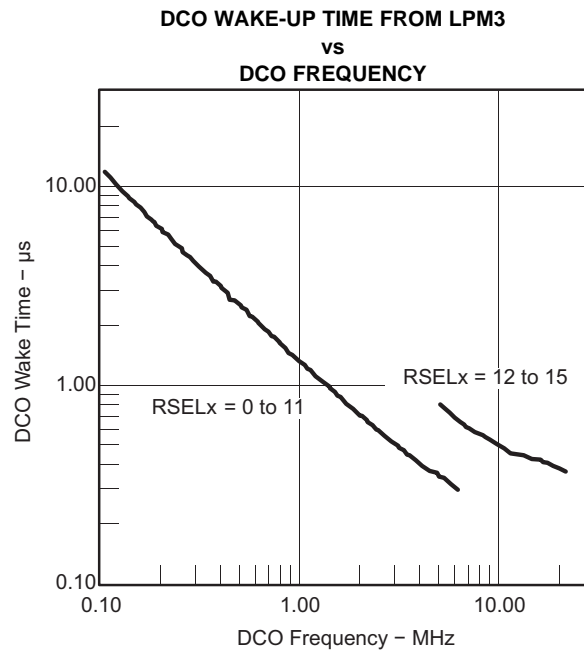


Figure 18.

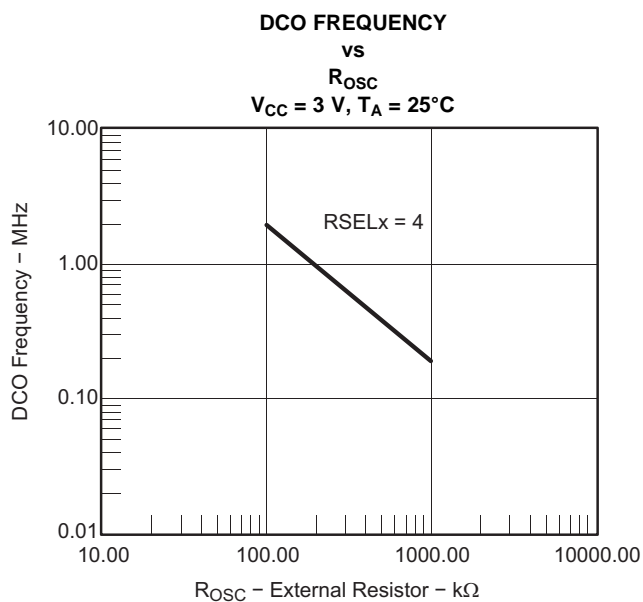
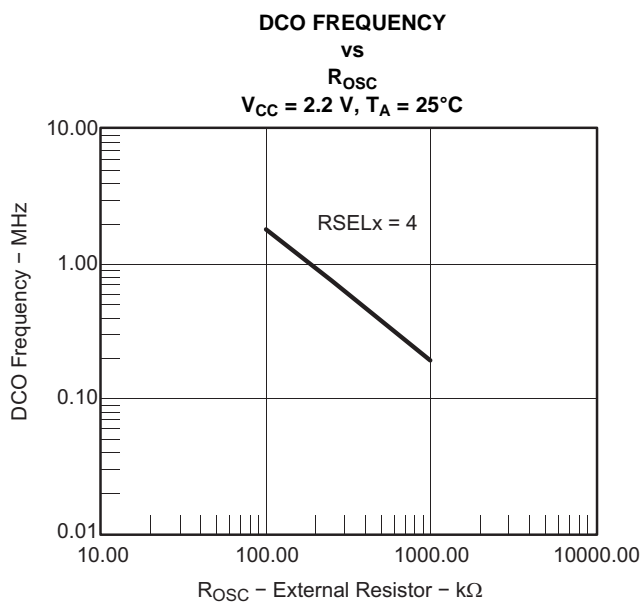
DCO With External Resistor R_{OSC} ⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | TYP | UNIT |
|--|---|------------|-----------|---------------|
| $f_{DCO,ROSC}$ DCO output frequency with R_{OSC} | DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0, $T_A = 25^\circ C$ | 2.2 V | 1.8 | MHz |
| | | 3 V | 1.95 | |
| D_T Temperature drift | DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0 | 2.2 V, 3 V | ± 0.1 | %/ $^\circ C$ |
| D_V Drift with V_{CC} | DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 10 | %/V |

(1) $R_{OSC} = 100\text{ k}\Omega$. Metal film resistor, type 0257, 0.6 W with 1% tolerance and $T_K = \pm 50\text{ ppm}/^\circ C$.

Typical Characteristics - DCO With External Resistor R_{OSC}



Typical Characteristics - DCO With External Resistor R_{OSC} (continued)

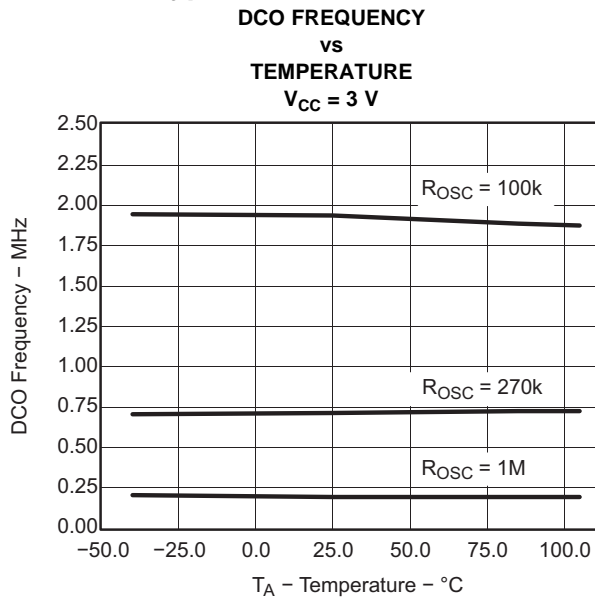


Figure 21.

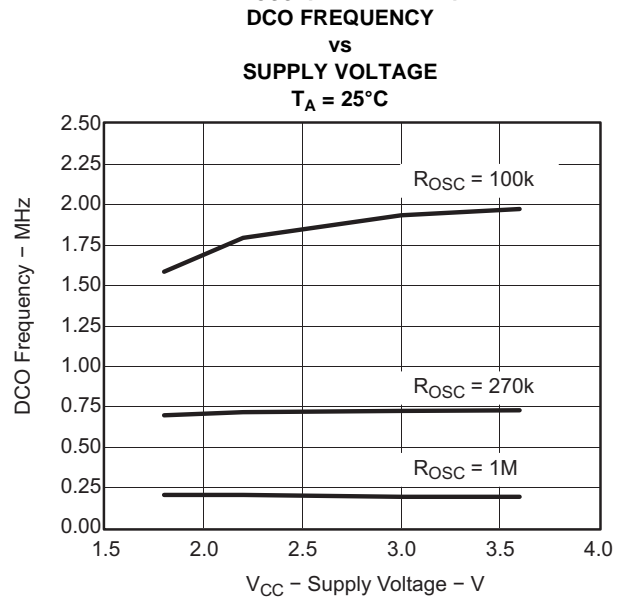


Figure 22.

Crystal Oscillator LFXT1, Low-Frequency Mode⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------------|---|--|-----------------|-------|-------|-------|------|
| f _{LFXT1,LF} | LFXT1 oscillator crystal frequency, LF mode 0, 1 | XTS = 0, LFXT1Sx = 0 or 1 | 1.8 V to 3.6 V | | 32768 | | Hz |
| f _{LFXT1,LF,logic} | LFXT1 oscillator logic level square wave input frequency, LF mode | XTS = 0, LFXT1Sx = 3, XCAPx = 0 | 1.8 V to 3.6 V | 10000 | 32768 | 50000 | Hz |
| O _{A,LF} | Oscillation allowance for LF crystals | XTS = 0, LFXT1Sx = 0, f _{LFXT1,LF} = 32768 Hz, C _{L,eff} = 6 pF | | | 500 | | kΩ |
| | | XTS = 0, LFXT1Sx = 0, f _{LFXT1,LF} = 32768 Hz, C _{L,eff} = 12 pF | | | 200 | | |
| C _{L,eff} | Integrated effective load capacitance, LF mode ⁽²⁾ | XTS = 0, XCAPx = 0 | | | 1 | | pF |
| | | XTS = 0, XCAPx = 1 | | | 5.5 | | |
| | | XTS = 0, XCAPx = 2 | | | 8.5 | | |
| | | XTS = 0, XCAPx = 3 | | | 11 | | |
| | Duty cycle, LF mode | XTS = 0, Measured at P2.0/ACLK, f _{LFXT1,LF} = 32768 Hz | 2.2 V, 3 V | 30 | 50 | 70 | % |
| f _{Fault,LF} | Oscillator fault frequency, LF mode ⁽³⁾ | XTS = 0, LFXT1Sx = 3, XCAPx = 0 ⁽⁴⁾ | 2.2 V, 3 V | 10 | | 10000 | Hz |

- (1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
 - (a) Keep the trace between the device and the crystal as short as possible.
 - (b) Design a good ground plane around the oscillator pins.
 - (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
 - (f) If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.
 - (g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
- (2) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the crystal that is used.
- (3) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
- (4) Measured with logic-level input frequency but also applies to operation with crystals.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | T _A | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------------------|---|----------------|-----------------|-----|-----|-----|------|
| f _{VLO} | VLO frequency | -40°C to 85°C | 2.2 V, 3 V | 4 | 12 | 20 | kHz |
| | | 105°C | | | | | |
| df _{VLO} /dT | VLO frequency temperature drift ⁽¹⁾ | | 2.2 V, 3 V | | 0.5 | | %/°C |
| df _{VLO} /dV _{CC} | VLO frequency supply voltage drift ⁽²⁾ | 25°C | 1.8 V to 3.6 V | | 4 | | %/V |

- (1) Calculated using the box method:
I: (MAX(-40 to 85°C) - MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C - (-40°C))
T: (MAX(-40 to 105°C) - MIN(-40 to 105°C)) / MIN(-40 to 105°C) / (105°C - (-40°C))
- (2) Calculated using the box method: (MAX(1.8 to 3.6 V) - MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V - 1.8 V)

Crystal Oscillator LFXT1, High-Frequency Mode⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------------|--|---|-----------------|------|-----|-----|------|
| f _{LFXT1,HF0} | LFXT1 oscillator crystal frequency, HF mode 0 | XTS = 1, LFXT1Sx = 0, XCAPx = 0 | 1.8 V to 3.6 V | 0.4 | | 1 | MHz |
| f _{LFXT1,HF1} | LFXT1 oscillator crystal frequency, HF mode 1 | XTS = 1, LFXT1Sx = 1, XCAPx = 0 | 1.8 V to 3.6 V | 1 | | 4 | MHz |
| f _{LFXT1,HF2} | LFXT1 oscillator crystal frequency, HF mode 2 | XTS = 1, LFXT1Sx = 2, XCAPx = 0 | 1.8 V to 3.6 V | 2 | | 10 | MHz |
| | | | 2.2 V to 3.6 V | 2 | | 12 | |
| | | | 3 V to 3.6 V | 2 | | 16 | |
| f _{LFXT1,HF,logic} | LFXT1 oscillator logic-level square-wave input frequency, HF mode | XTS = 1, LFXT1Sx = 3, XCAPx = 0 | 1.8 V to 3.6 V | 0.4 | | 10 | MHz |
| | | | 2.2 V to 3.6 V | 0.4 | | 12 | |
| | | | 3 V to 3.6 V | 0.4 | | 16 | |
| OA _{HF} | Oscillation allowance for HF crystals (see Figure 23 and Figure 24) | XTS = 1, XCAPx = 0, LFXT1Sx = 0, f _{LFXT1,HF} = 1 MHz, C _{L,eff} = 15 pF | | 2700 | | | Ω |
| | | XTS = 1, XCAPx = 0, LFXT1Sx = 1, f _{LFXT1,HF} = 4 MHz, C _{L,eff} = 15 pF | | 800 | | | |
| | | XTS = 1, XCAPx = 0, LFXT1Sx = 2, f _{LFXT1,HF} = 16 MHz, C _{L,eff} = 15 pF | | 300 | | | |
| C _{L,eff} | Integrated effective load capacitance, HF mode ⁽²⁾ | XTS = 1, XCAPx = 0 ⁽³⁾ | | 1 | | | pF |
| | Duty cycle, HF mode | XTS = 1, XCAPx = 0, Measured at P2.0/ACLK, f _{LFXT1,HF} = 10 MHz | 2.2 V, 3 V | 40 | 50 | 60 | % |
| | | XTS = 1, XCAPx = 0, Measured at P2.0/ACLK, f _{LFXT1,HF} = 16 MHz | | 40 | 50 | 60 | |
| f _{Fault,HF} | Oscillator fault frequency ⁽⁴⁾ | XTS = 1, LFXT1Sx = 3, XCAPx = 0 ⁽⁵⁾ | 2.2 V, 3 V | 30 | | 300 | kHz |

- (1) To improve EMI on the XT2 oscillator the following guidelines should be observed:
 - (a) Keep the trace between the device and the crystal as short as possible.
 - (b) Design a good ground plane around the oscillator pins.
 - (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
 - (f) If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.
 - (g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
- (2) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (3) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
- (4) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.
- (5) Measured with logic-level input frequency, but also applies to operation with crystals.

Typical Characteristics - LFXT1 Oscillator in HF Mode (XTS = 1)

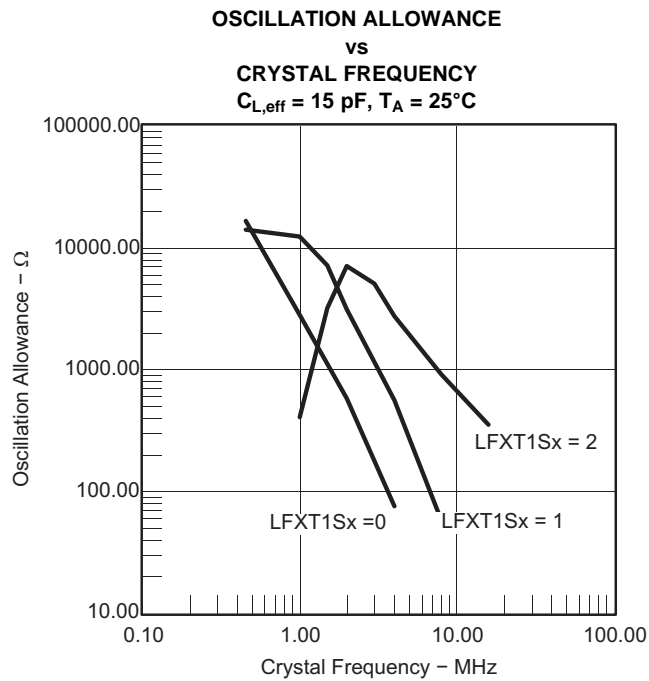


Figure 23.

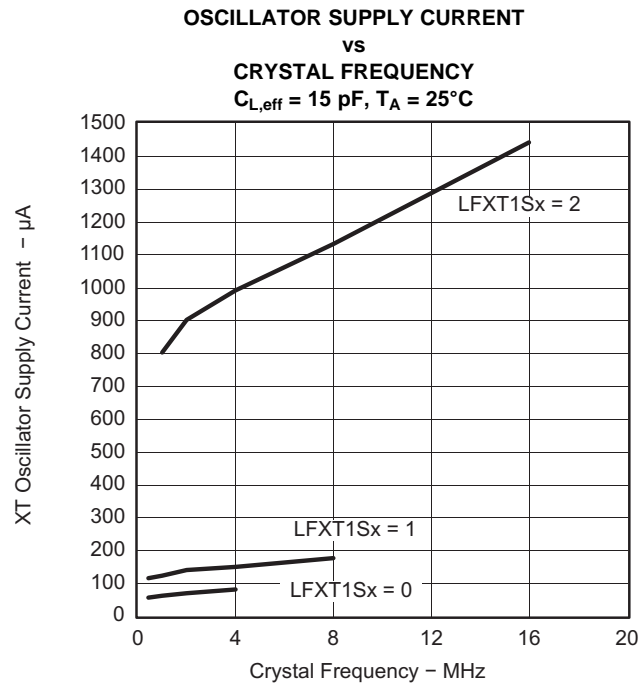


Figure 24.

Crystal Oscillator XT2⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--------------------|---|--|-----------------|-----|------|-----|------|
| f _{XT2} | XT2 oscillator crystal frequency, mode 0 | XT2Sx = 0 | 1.8 V to 3.6 V | 0.4 | | 1 | MHz |
| f _{XT2} | XT2 oscillator crystal frequency, mode 1 | XT2Sx = 1 | 1.8 V to 3.6 V | 1 | | 4 | MHz |
| f _{XT2} | XT2 oscillator crystal frequency, mode 2 | XT2Sx = 2 | 1.8 V to 2.2 V | 2 | | 10 | MHz |
| | | | 2.2 V to 3.6 V | 2 | | 12 | |
| | | | 3 V to 3.6 V | 2 | | 16 | |
| f _{XT2} | XT2 oscillator logic-level square-wave input frequency | XT2Sx = 3 | 1.8 V to 2.2 V | 0.4 | | 10 | MHz |
| | | | 2.2 V to 3.6 V | 0.4 | | 12 | |
| | | | 3 V to 3.6 V | 0.4 | | 16 | |
| OA | Oscillation allowance (see Figure 25 and Figure 26) | XT2Sx = 0, f _{XT2} = 1 MHz, C _{L,eff} = 15 pF | | | 2700 | | Ω |
| | | XT2Sx = 1, f _{XT2} = 4 MHz, C _{L,eff} = 15 pF | | | 800 | | |
| | | XT2Sx = 2, f _{XT2} = 16 MHz, C _{L,eff} = 15 pF | | | 300 | | |
| C _{L,eff} | Integrated effective load capacitance, HF mode ⁽²⁾ | See ⁽³⁾ | | | 1 | | pF |
| | Duty cycle | Measured at P1.4/SMCLK, f _{XT2} = 10 MHz | 2.2 V, 3 V | 40 | 50 | 60 | % |
| | | Measured at P1.4/SMCLK, f _{XT2} = 16 MHz | | 40 | 50 | 60 | |
| f _{Fault} | Oscillator fault frequency, HF mode ⁽⁴⁾ | XT2Sx = 3 ⁽⁵⁾ | 2.2 V, 3 V | 30 | | 300 | kHz |

- (1) To improve EMI on the XT2 oscillator the following guidelines should be observed:
 - (a) Keep the trace between the device and the crystal as short as possible.
 - (b) Design a good ground plane around the oscillator pins.
 - (c) Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
 - (d) Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
 - (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
 - (f) If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (3) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
- (4) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.
- (5) Measured with logic-level input frequency, but also applies to operation with crystals.

Typical Characteristics - XT2 Oscillator

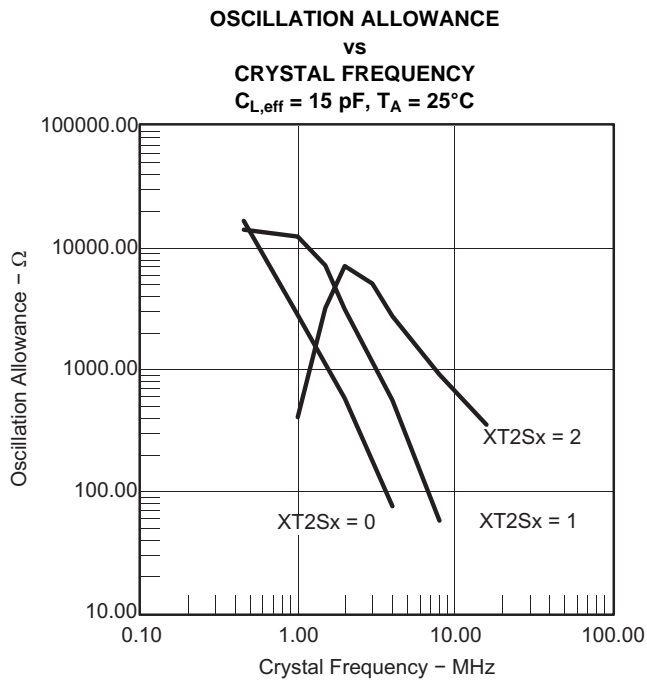


Figure 25.

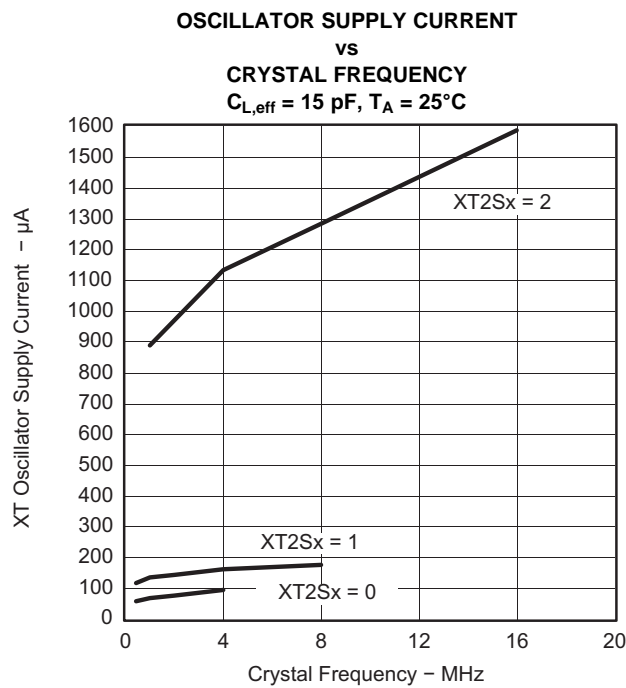


Figure 26.

Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|-------------------------|---|-----------------|-----|-----|-----|------|
| f _{TA} | Timer_A clock frequency | Internal: SMCLK, ACLK External: TACLK, INCLK Duty cycle = 50% ± 10% | 2.2 V | | | 10 | MHz |
| | | | 3 V | | | 16 | |
| t _{TA,cap} | Timer_A capture timing | TA0, TA1, TA2 | 2.2 V, 3 V | 20 | | | ns |

Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|-------------------------|---|-----------------|-----|-----|-----|------|
| f _{TB} | Timer_B clock frequency | Internal: SMCLK, ACLK External: TACLK, INCLK Duty cycle = 50% ± 10% | 2.2 V | | | 10 | MHz |
| | | | 3 V | | | 16 | |
| t _{TB,cap} | Timer_B capture timing | TB0, TB1, TB2 | 2.2 V, 3 V | 20 | | | ns |

USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|--|---|-----------------|---------------------|-----|-----|------|
| f _{USCI} | USCI input clock frequency | Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10% | | f _{SYSTEM} | | | MHz |
| f _{BITCLK} | BITCLK clock frequency (equals baud rate in Mbaud) ⁽¹⁾ | | 2.2 V, 3 V | 1 | | | MHz |
| t _r | UART receive deglitch time ⁽²⁾ | | 2.2 V | 50 | 150 | 600 | ns |
| | | | 3 V | 50 | 100 | 600 | |

(1) The DCO wake-up time must be considered in LPM3 or LPM4 for baud rates above 1 MHz.

(2) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed.

USCI (SPI Master Mode)⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

(see [Figure 27](#) and [Figure 28](#))

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------------|-----------------------------|---|-----------------|---------------------|-----|------|
| f _{USCI} | USCI input clock frequency | SMCLK, ACLK Duty cycle = 50% ± 10% | | f _{SYSTEM} | | MHz |
| t _{SU,MI} | SOMI input data setup time | | 2.2 V | 110 | | ns |
| | | | 3 V | 75 | | |
| t _{HD,MI} | SOMI input data hold time | | 2.2 V | 0 | | ns |
| | | | 3 V | 0 | | |
| t _{VALID,MO} | SIMO output data valid time | UCLK edge to SIMO valid, C _L = 20 pF | 2.2 V | | 30 | ns |
| | | | 3 V | | 20 | |

(1) f_{UCxCLK} = 1/2t_{LO/HI} with t_{LO/HI} ≥ max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)}).

For the slave's parameters t_{SU,SI(Slave)} and t_{VALID,SO(Slave)}, see the SPI parameters of the attached slave.

USCI (SPI Slave Mode)⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

(see [Figure 29](#) and [Figure 30](#))

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|---|--|-----------------|-----|-----|-----|------|
| t _{STE,LEAD} | STE lead time, STE low to clock | | 2.2 V, 3 V | 50 | | | ns |
| t _{STE,LAG} | STE lag time, Last clock to STE high | | 2.2 V, 3 V | 10 | | | ns |
| t _{STE,ACC} | STE access time, STE low to SOMI data out | | 2.2 V, 3 V | 50 | | | ns |
| t _{STE,DIS} | STE disable time, STE high to SOMI high impedance | | 2.2 V, 3 V | 50 | | | ns |
| t _{SU,SI} | SIMO input data setup time | | 2.2 V | 20 | | | ns |
| | | | 3 V | 15 | | | |
| t _{HD,SI} | SIMO input data hold time | | 2.2 V | 10 | | | ns |
| | | | 3 V | 10 | | | |
| t _{VALID,SO} | SOMI output data valid time | UCLK edge to SOMI valid, C _L = 20 pF | 2.2 V | 75 | 110 | | ns |
| | | | 3 V | 50 | 75 | | |

(1) f_{UCxCLK} = 1/2t_{LO/HI} with t_{LO/HI} ≥ max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)}).

For the master's parameters t_{SU,MI(Master)} and t_{VALID,MO(Master)} see the SPI parameters of the attached slave.

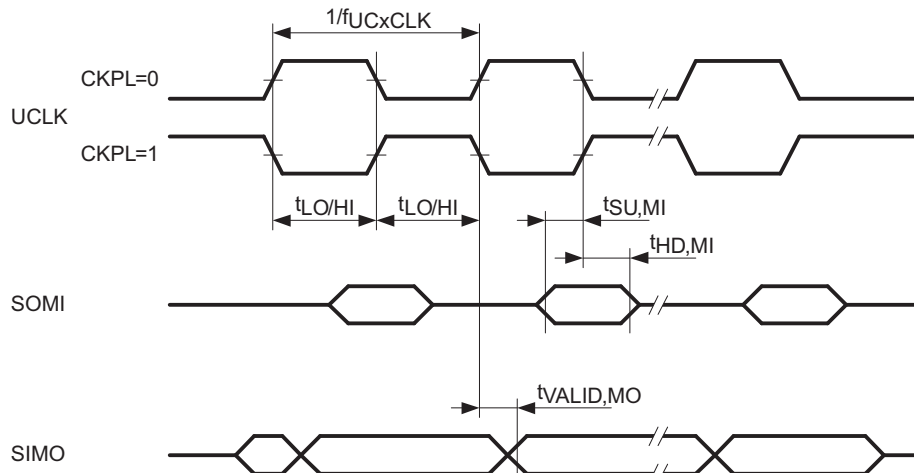


Figure 27. SPI Master Mode, CKPH = 0

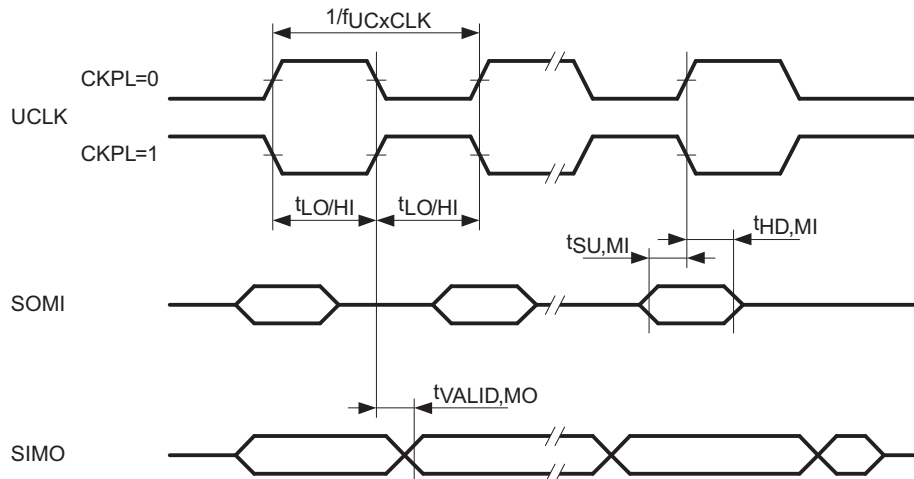


Figure 28. SPI Master Mode, CKPH = 1

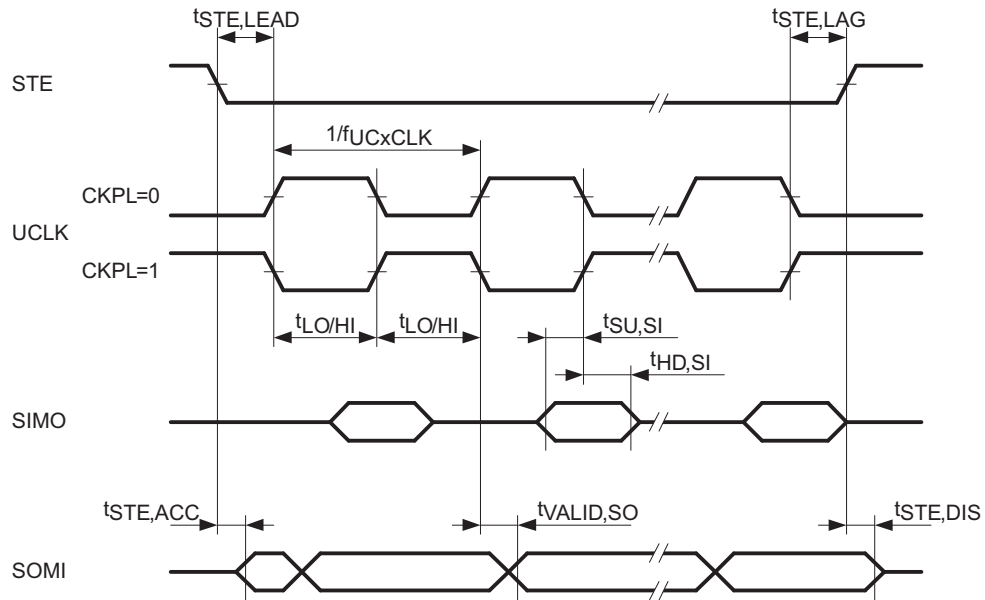


Figure 29. SPI Slave Mode, CKPH = 0

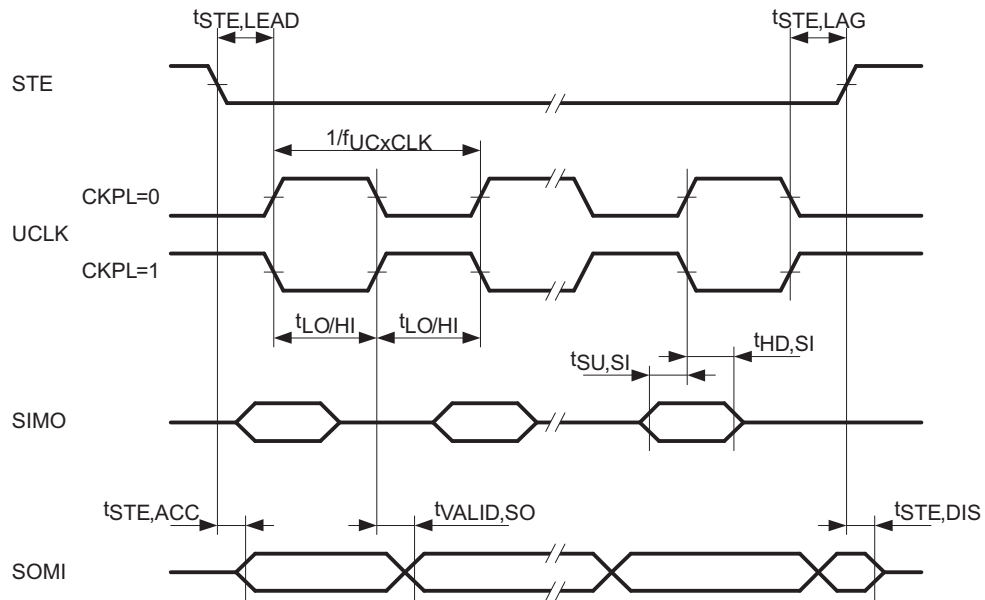


Figure 30. SPI Slave Mode, CKPH = 1

USCI (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 31](#))

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|---|--|------------|------------|---------------------|------|
| f _{USCI} | USCI input clock frequency | | | | f _{SYSTEM} | MHz |
| f _{SCL} | SCL clock frequency | 2.2 V, 3 V | 0 | | 400 | kHz |
| t _{HD,STA} | Hold time (repeated) START | f _{SCL} ≤ 100 kHz f _{SCL} > 100 kHz | 2.2 V, 3 V | 4 0.6 | | μs |
| t _{SU,STA} | Setup time for a repeated START | f _{SCL} ≤ 100 kHz f _{SCL} > 100 kHz | 2.2 V, 3 V | 4.7 0.6 | | μs |
| t _{HD,DAT} | Data hold time | | 2.2 V, 3 V | 0 | | ns |
| t _{SU,DAT} | Data setup time | | 2.2 V, 3 V | 250 | | ns |
| t _{SU,STO} | Setup time for STOP | | 2.2 V, 3 V | 4 | | μs |
| t _{SP} | Pulse duration of spikes suppressed by input filter | 2.2 V 3 V | 50 50 | 150 100 | 600 600 | ns |

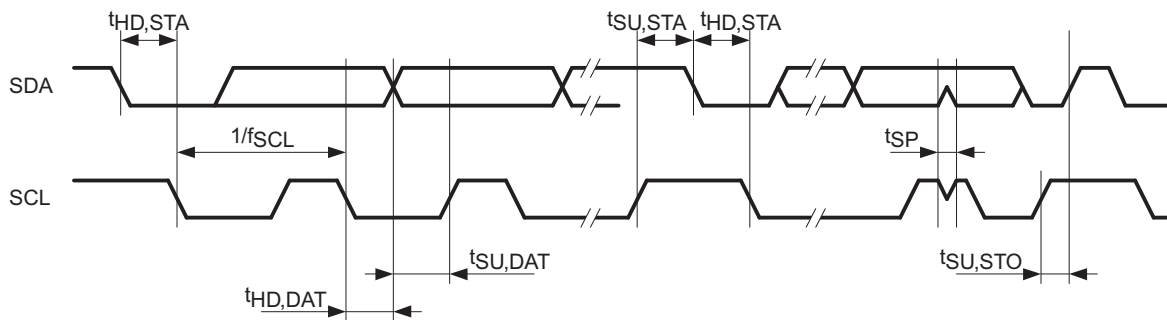


Figure 31. I²C Mode Timing

Comparator_A+⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|-----------------------------------|--|--|-------|------|---------------------|------|----|
| I _(DD) | CAON = 1, CARSEL = 0, CAREF = 0 | 2.2 V | | 25 | 40 | μA | |
| | | 3 V | | 45 | 60 | | |
| I _(Refladder/RefDiode) | CAON = 1, CARSEL = 0, CAREF = 1/2/3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2 | 2.2 V | | 30 | 50 | μA | |
| | | 3 V | | 45 | 71 | | |
| V _{IC} | Common-mode input voltage range CAON = 1 | 2.2 V, 3 V | 0 | | V _{CC} - 1 | V | |
| V _(Ref025) | (Voltage at 0.25 V _{CC} node) ÷ V _{CC} PCA0 = 1, CARSEL = 1, CAREF = 1, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2 | 2.2 V, 3 V | 0.23 | 0.24 | 0.25 | | |
| V _(Ref050) | (Voltage at 0.5 V _{CC} node) ÷ V _{CC} PCA0 = 1, CARSEL = 1, CAREF = 2, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2 | 2.2 V, 3 V | 0.47 | 0.48 | 0.5 | | |
| V _(RefVT) | See Figure 35 and Figure 36 PCA0 = 1, CARSEL = 1, CAREF = 3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2, T _A = 85°C | 2.2 V | 390 | 480 | 540 | mV | |
| | | 3 V | 400 | 490 | 550 | | |
| V _(offset) | Offset voltage ⁽²⁾ | 2.2 V, 3 V | -30 | | 30 | mV | |
| V _{hys} | Input hysteresis CAON = 1 | 2.2 V, 3 V | 0 | 0.7 | 1.4 | mV | |
| t _(response) | Response time, low to high and high to low ⁽³⁾ (see Figure 32 and Figure 33) | T _A = 25°C, Overdrive 10 mV, Without filter: CAF = 0 | 2.2 V | 80 | 165 | 300 | ns |
| | | | 3 V | 70 | 120 | 240 | |
| | | T _A = 25°C, Overdrive 10 mV, With filter: CAF = 1 | 2.2 V | 1.4 | 1.9 | 2.8 | μs |
| | | | 3 V | 0.9 | 1.5 | 2.2 | |

- (1) The leakage current for the Comparator_A+ terminals is identical to I_{lkg(Px,y)} specification.
- (2) The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A+ inputs on successive measurements. The two successive measurements are then summed together.
- (3) The response time is measured at P2.2/CAOUT/TA0/CA4 with an input voltage step and with Comparator_A+ already enabled (CAON = 1). If CAON is set at the same time, a settling time of up to 300 ns is added to the response time.

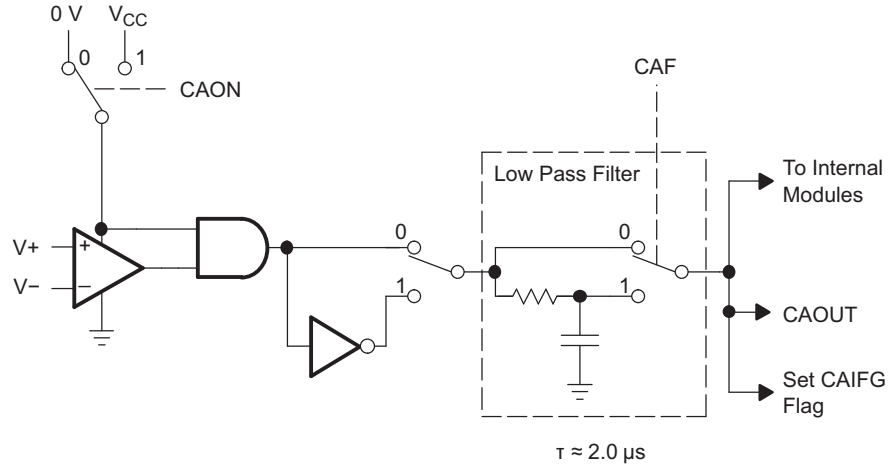


Figure 32. Comparator_A+ Module Block Diagram

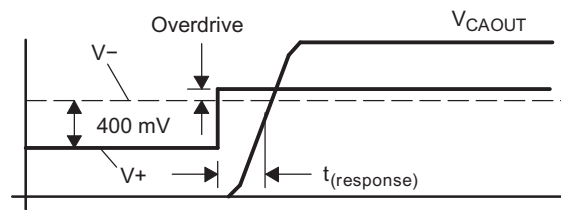


Figure 33. Overdrive Definition

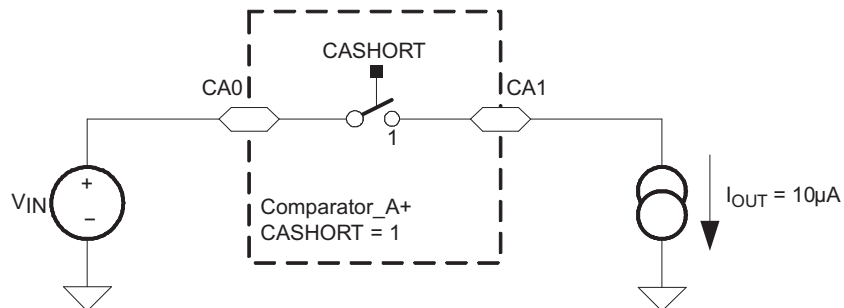


Figure 34. Comparator_A+ Short Resistance Test Condition

Typical Characteristics, Comparator_A+

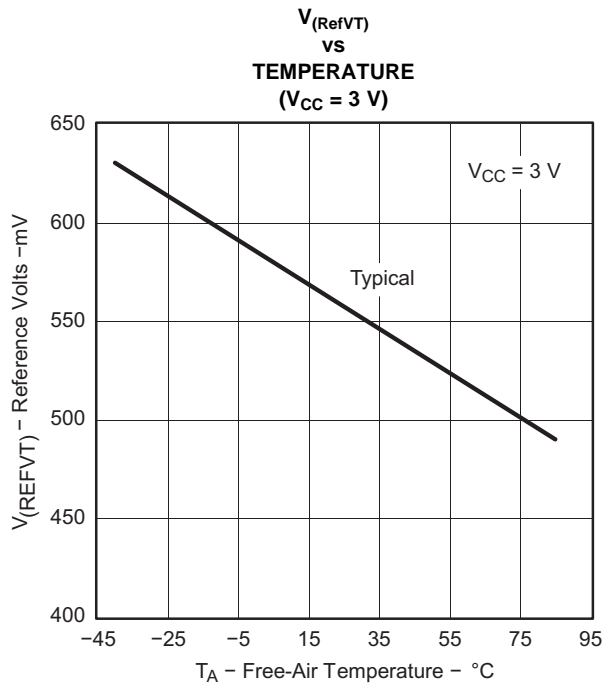


Figure 35.

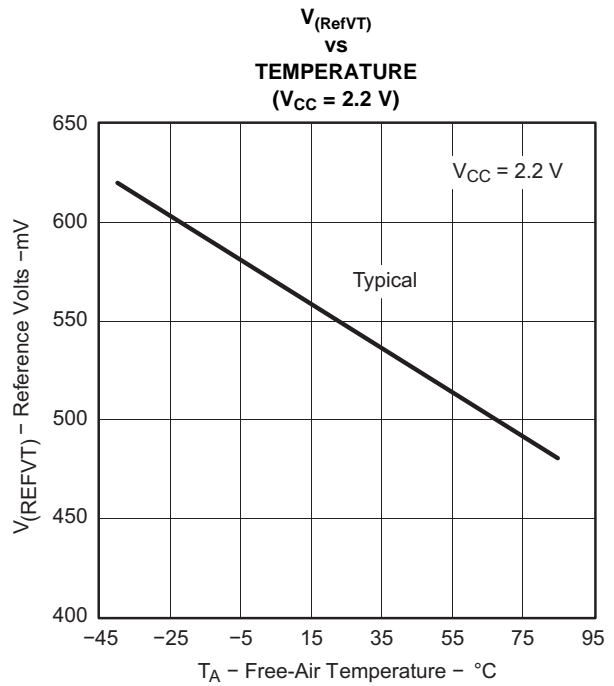


Figure 36.

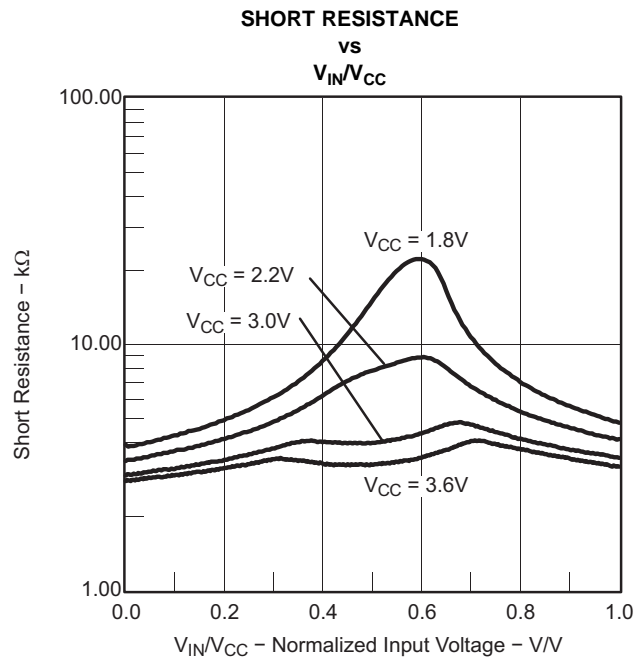


Figure 37.

12-Bit ADC Power Supply and Input Range Conditions ⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---|---|-----------------|-----|------|-------------------|------|
| AV _{CC} Analog supply voltage | AV _{CC} and DV _{CC} are connected together, AV _{SS} and DV _{SS} are connected together, V _(AVSS) = V _(DVSS) = 0 V | | 2.2 | | 3.6 | V |
| V _(P6.x/Ax) Analog input voltage range ⁽²⁾ | All P6.0/A0 to P6.7/A7 terminals, Analog inputs selected in ADC12MCTLx register, P6Sel.x = 1, 0 ≤ x ≤ 7, V _(AVSS) ≤ V _{P6.x/Ax} ≤ V _(AVCC) | | 0 | | V _{AVCC} | V |
| I _{ADC12} Operating supply current into AV _{CC} terminal ⁽³⁾ | f _{ADC12CLK} = 5 MHz, ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0 | 2.2 V | | 0.65 | 0.8 | mA |
| | | 3 V | | 0.8 | 1 | |
| I _{REF+} Operating supply current into AV _{CC} terminal ⁽⁴⁾ | f _{ADC12CLK} = 5 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 1 | 3 V | | 0.5 | 0.7 | mA |
| | f _{ADC12CLK} = 5 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 0 | 2.2 V | | 0.5 | 0.7 | |
| | | 3 V | | 0.5 | 0.7 | mA |
| C _I Input capacitance ⁽⁵⁾ | Only one terminal can be selected at one time, P6.x/Ax | 2.2 V | | | 40 | |
| R _I Input MUX ON resistance ⁽⁵⁾ | 0 V ≤ V _{Ax} ≤ V _{AVCC} | 3 V | | | 2000 | Ω |

- (1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.
- (2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
- (3) The internal reference supply current is not included in current consumption parameter I_{ADC12}.
- (4) The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables settling of the built-in reference before starting an A/D conversion.
- (5) Not production tested, limits verified by design.

12-Bit ADC External Reference ⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|--|--|-----------------|-----|-------------------|------|
| V _{eREF+} Positive external reference voltage input | V _{eREF+} > V _{REF} /V _{eREF-} ⁽²⁾ | | 1.4 | V _{AVCC} | V |
| V _{REF} /V _{eREF-} Negative external reference voltage input | V _{eREF+} > V _{REF} /V _{eREF-} ⁽³⁾ | | 0 | 1.2 | V |
| (V _{eREF+} - V _{REF-})/V _{eREF-} Differential external reference voltage input | V _{eREF+} > V _{REF} /V _{eREF-} ⁽⁴⁾ | | 1.4 | V _{AVCC} | V |
| I _{VeREF+} Static leakage current | 0 V ≤ V _{eREF+} ≤ V _{AVCC} | 2.2 V, 3 V | | ±1 | μA |
| I _{VREF-/VeREF-} Static leakage current | 0 V ≤ V _{eREF-} ≤ V _{AVCC} | 2.2 V, 3 V | | ±1 | μA |

- (1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
- (2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
- (3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
- (4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

12-Bit ADC Built-In Reference

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T _A | V _{CC} | MIN | NOM | MAX | UNIT | |
|------------------------|--|--|-----------------|---------------|-----|------|--------|---|
| V _{REF+} | Positive built-in reference voltage output | REF2_5V = 1 for 2.5 V, I _{VREF+} max ≤ I _{VREF+} ≤ I _{VREF+} min | 3 V | -40°C to 85°C | 2.4 | 2.5 | 2.6 | V |
| | | 105°C | | 2.37 | 2.5 | 2.64 | | |
| | REF2_5V = 0 for 1.5 V, I _{VREF+} max ≤ I _{VREF+} ≤ I _{VREF+} min | 2.2 V, 3 V | -40°C to 85°C | 1.44 | 1.5 | 1.56 | | |
| | | | 105°C | 1.42 | 1.5 | 1.57 | | |
| AV _{CC(min)} | AV _{CC} minimum voltage, positive built-in reference active | REF2_5V = 0, I _{VREF+} max ≤ I _{VREF+} ≤ I _{VREF+} min | | | 2.2 | | V | |
| | | REF2_5V = 1, -0.5 mA ≤ I _{VREF+} ≤ I _{VREF+} min | | | 2.8 | | | |
| | | REF2_5V = 1, -1 mA ≤ I _{VREF+} ≤ I _{VREF+} min | | | 2.9 | | | |
| I _{VREF+} | Load current out of V _{REF+} terminal | | 2.2 V | 0.01 | | -0.5 | mA | |
| | | | 3 V | 0.01 | | -1 | | |
| I _{L(VREF+)} | Load-current regulation, V _{REF+} terminal ⁽¹⁾ | I _{VREF+} = 500 μA ± 100 μA, Analog input voltage ≈ 0.75 V, REF2_5V = 0 | 2.2 V | | | ±2 | LSB | |
| | | | 3 V | | | ±2 | | |
| | | I _{VREF+} = 500 μA ± 100 μA, Analog input voltage ≈ 1.25 V, REF2_5V = 1 | 3 V | | | ±2 | LSB | |
| I _{DL(VREF+)} | Load current regulation, V _{REF+} terminal ⁽²⁾ | I _{VREF+} = 100 μA → 900 μA, C _{VREF+} = 5 μF, ax ≈ 0.5 × V _{REF+} , Error of conversion result ≤ 1 LSB | 3 V | | | 20 | ns | |
| C _{VREF+} | Capacitance at pin V _{REF+} ⁽³⁾ | REFON = 1, 0 mA ≤ I _{VREF+} ≤ I _{VREF+} max | 2.2 V, 3 V | 5 | 10 | | μF | |
| T _{REF+} | Temperature coefficient of built-in reference ⁽²⁾ | I _{VREF+} is a constant in the range of 0 mA ≤ I _{VREF+} ≤ 1 mA | 2.2 V, 3 V | | | ±100 | ppm/°C | |
| t _{REFON} | Settle time of internal reference voltage (see Figure 38) ⁽⁴⁾ ⁽²⁾ | I _{VREF+} = 0.5 mA, C _{VREF+} = 10 μF, V _{REF+} = 1.5 V, V _{AVCC} = 2.2 V | 2.2 V | | | 17 | ms | |

(1) Not production tested, limits characterized.

(2) Not production tested, limits verified by design.

(3) The internal buffer operational amplifier and the accuracy specifications require an external capacitor. All INL and DNL tests uses two capacitors between pins V_{REF+} and AV_{SS} and V_{REF-}/V_{REF-} and AV_{SS}: 10 μF tantalum and 100 nF ceramic.

(4) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load.

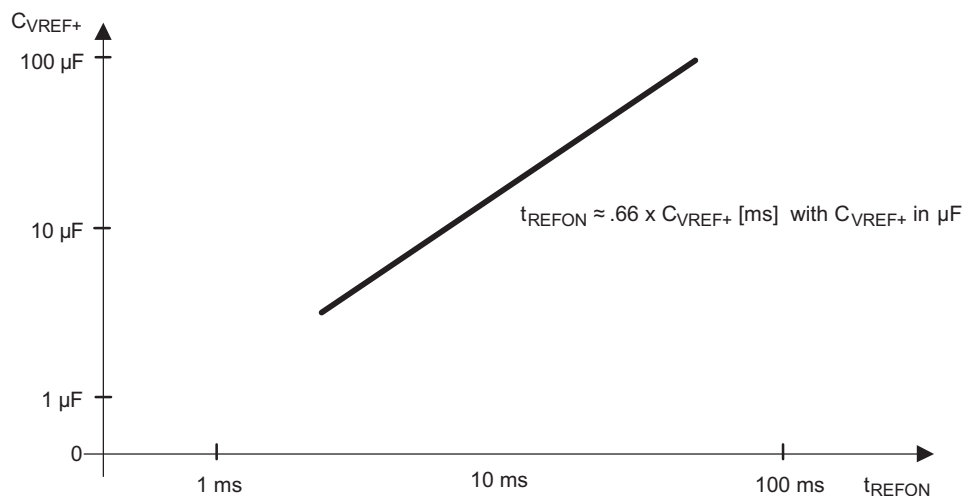


Figure 38. Typical Settling Time of Internal Reference t_{REFON} vs External Capacitor on V_{REF+}

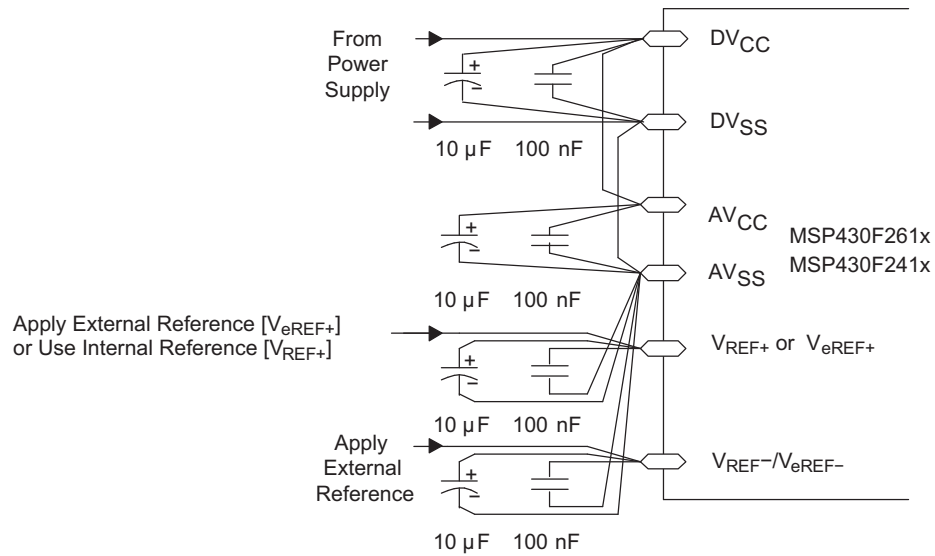


Figure 39. Supply Voltage and Reference Voltage Design V_{REF-}/V_{eREF-} External Supply

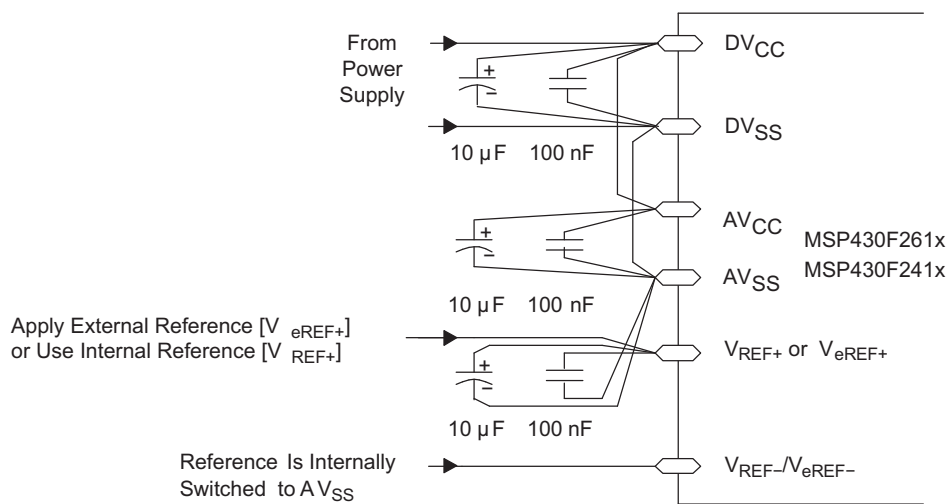


Figure 40. Supply Voltage and Reference Voltage Design $V_{REF-}/V_{eREF-} = AV_{SS}$, Internally Connected

12-Bit ADC Timing Parameters

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|--|--------------------|------|---|------|------|
| f _{ADC12CLK} | For specified performance of ADC12 linearity parameters | 2.2 V, 3 V | 0.45 | 5 | 6.3 | MHz |
| f _{ADC12OSC} | Internal ADC12 oscillator ADC12DIV = 0, f _{ADC12CLK} = f _{ADC12OSC} | 2.2 V, 3 V | 3.7 | 5 | 6.3 | MHz |
| t _{CONVERT} | C _{VREF+} ≥ 5 μF, Internal oscillator, f _{ADC12OSC} = 3.7 MHz to 6.3 MHz | 2.2 V, 3 V | 2.06 | | 3.51 | μs |
| | External f _{ADC12CLK} from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0 | | | 13 × ADC12DIV × 1/f _{ADC12CLK} | | μs |
| t _{ADC12ON} | Turn-on settling time of the ADC ⁽¹⁾ | See ⁽²⁾ | | | 100 | ns |
| t _{Sample} | Sampling time ⁽¹⁾ R _S = 400 Ω, R _I = 1000 Ω, C _I = 30 pF, τ = [R _S + R _I] × C _I ⁽³⁾ | 3 V | 1220 | | | ns |
| | | 2.2 V | 1400 | | | |

(1) Limits verified by design

(2) The condition is that the error in a conversion started after t_{ADC12ON} is less than ±0.5 LSB. The reference and input signal are already settled.

(3) Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:

t_{sample} = ln(2ⁿ⁺¹) × (R_S + R_I) × C_I + 800 ns, where n = ADC resolution = 12, R_S = external source resistance

12-Bit ADC Linearity Parameters

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------|--|-----------------|-----|------|------|------|
| E _I | 1.4 V ≤ (V _{eREF+} - V _{REF-/V_{eREF-}}) min ≤ 1.6 V | 2.2 V, 3 V | | | ±2 | LSB |
| | 1.6 V < (V _{eREF+} - V _{REF-/V_{eREF-}}) min ≤ V _{AVCC} | | | | ±1.7 | |
| E _D | (V _{eREF+} - V _{REF-/V_{eREF-}}) min ≤ (V _{eREF+} - V _{REF-/V_{eREF-}}), C _{VREF+} = 10 μF (tantalum) and 100 nF (ceramic) | 2.2 V, 3 V | | | ±1 | LSB |
| E _O | (V _{eREF+} - V _{REF-/V_{eREF-}}) min ≤ (V _{eREF+} - V _{REF-/V_{eREF-}}), Internal impedance of source R _S < 100 Ω, C _{VREF+} = 10 μF (tantalum) and 100 nF (ceramic) | 2.2 V, 3 V | | ±2 | ±4 | LSB |
| E _G | (V _{eREF+} - V _{REF-/V_{eREF-}}) min ≤ (V _{eREF+} - V _{REF-/V_{eREF-}}), C _{VREF+} = 10 μF (tantalum) and 100 nF (ceramic) | 2.2 V, 3 V | | ±1.1 | ±2 | LSB |
| E _T | (V _{eREF+} - V _{REF-/V_{eREF-}}) min ≤ (V _{eREF+} - V _{REF-/V_{eREF-}}), C _{VREF+} = 10 μF (tantalum) and 100 nF (ceramic) | 2.2 V, 3 V | | ±2 | ±5 | LSB |

12-Bit ADC Temperature Sensor and Built-In V_{MID}

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|-------------------------------------|---|---|----------|-----|------|-------------------|----------------|
| I_{SENSOR} | Operating supply current into AV_{CC} terminal ⁽¹⁾ | REFON = 0, INCH = 0Ah, ADC12ON = 1, $T_A = 25^\circ C$ | 2.2 V | | 40 | 120 | μA |
| | | | 3V | | 60 | 160 | |
| V_{SENSOR} ^{(2) (3)} | | ADC12ON = 1, INCH = 0Ah, $T_A = 0^\circ C$ | 2.2 V | | 986 | | mV |
| | | | 3V | | 986 | | |
| TC_{SENSOR} ⁽³⁾ | | ADC12ON = 1, INCH = 0Ah | 2.2 V | | 3.55 | | mV/ $^\circ C$ |
| | | | 3V | | 3.55 | | |
| $t_{SENSOR(sample)}$ ⁽³⁾ | Sample time required if channel 10 is selected ⁽⁴⁾ | ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB | 2.2 V | | 30 | | μs |
| | | | 3V | | 30 | | |
| I_{VMID} | Current into divider at channel 11 ⁽⁵⁾ | ADC12ON = 1, INCH = 0Bh | 2.2 V | | | NA ⁽⁵⁾ | μA |
| | | | 3V | | | NA ⁽⁵⁾ | |
| V_{MID} | AV_{CC} divider at channel 11 | ADC12ON = 1, INCH = 0Bh, V_{MID} is approximately $0.5 \times V_{AVCC}$ | 2.2 V | | 1.1 | 1.1 ± 0.04 | V |
| | | | 3V | | 1.5 | 1.5 ± 0.04 | |
| $t_{VMID(sample)}$ | Sample time required if channel 11 is selected ⁽⁶⁾ | ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB | 2.2 V | | 1400 | | ns |
| | | | 3 V | | 1220 | | |

- (1) The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and REFON = 1), or (ADC12ON = 1 AND INCH = 0Ah and sample signal is high). Therefore it includes the constant current through the sensor and the reference.
- (2) The temperature sensor offset can be as much as $\pm 20^\circ C$. A single-point calibration is recommended to minimize the offset error of the built-in temperature sensor.
- (3) Limits characterized
- (4) The typical equivalent impedance of the sensor is 51 k Ω . The sample time required includes the sensor-on time $t_{SENSOR(on)}$
- (5) No additional current is needed. The V_{MID} is used during sampling.
- (6) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$, no additional on time is needed.

12-Bit DAC Supply Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CC} | T_A | MIN | TYP | MAX | UNIT |
|-----------|--|---|------------|---------------------------------|-----|-----|------|---------|
| AV_{CC} | Analog supply voltage | $AV_{CC} = DV_{CC}$, $AV_{SS} = DV_{SS} = 0 V$ | | | 2.2 | | 3.6 | V |
| I_{DD} | Supply current, single DAC channel ⁽¹⁾⁽²⁾ | DAC12AMPx = 2, DAC12IR = 0, DAC12_xDAT = 0x0800 | 2.2 V, 3 V | -40 $^\circ C$ to 85 $^\circ C$ | | 50 | 110 | μA |
| | | | | | | 69 | 150 | |
| | | DAC12AMPx = 2, DAC12IR = 1, DAC12_xDAT = 0x0800, $V_{eREF+} = V_{REF+} = AV_{CC}$ | 2.2 V, 3 V | | | 50 | 130 | |
| | | DAC12AMPx = 5, DAC12IR = 1, DAC12_xDAT = 0x0800, $V_{eREF+} = V_{REF+} = AV_{CC}$ | 2.2 V, 3 V | | | 200 | 440 | |
| | | DAC12AMPx = 7, DAC12IR = 1, DAC12_xDAT = 0x0800, $V_{eREF+} = V_{REF+} = AV_{CC}$ | 2.2 V, 3 V | | | 700 | 1500 | |
| PSRR | Power-supply rejection ratio ⁽³⁾⁽⁴⁾ | DAC12_xDAT = 800h, $V_{REF} = 1.5 V$, $\Delta AV_{CC} = 100 mV$ | 2.2 V | | | 70 | | dB |
| | | DAC12_xDAT = 800h, $V_{REF} = 1.5 V$ or 2.5 V, $\Delta AV_{CC} = 100 mV$ | 3 V | | | 70 | | |

- (1) No load at the output pin, DAC12_0 or DAC12_1, assuming that the control bits for the shared pins are set properly.
- (2) Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Reference Input specifications.
- (3) $PSRR = 20 \times \log(\Delta AV_{CC} / \Delta V_{DAC12_xOUT})$
- (4) V_{REF} is applied externally. The internal reference is not used.

12-Bit DAC Linearity Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------|--|---|-----------------|-----|------|-------|---------------|
| Resolution | | 12-bit monotonic | | 12 | | | bits |
| INL | Integral nonlinearity ⁽¹⁾ | V _{REF} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1 | 2.2 V | | ±2.0 | ±8.0 | LSB |
| | | V _{REF} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1 | 3 V | | | | |
| DNL | Differential nonlinearity ⁽¹⁾ | V _{REF} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1 | 2.2 V | | ±0.4 | ±1.0 | LSB |
| | | V _{REF} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1 | 3 V | | | | |
| E _O | Offset voltage without calibration ⁽¹⁾⁽²⁾ | V _{REF} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1 | 2.2 V | | | ±21 | mV |
| | | V _{REF} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1 | 3 V | | | | |
| | Offset voltage with calibration ⁽¹⁾⁽²⁾ | V _{REF} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1 | 2.2 V | | | ±2.5 | |
| | | V _{REF} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1 | 3 V | | | | |
| d _{E(O)/dT} | Offset error temperature coefficient ⁽³⁾ | | 2.2 V, 3 V | | 30 | | µV/C |
| E _G | Gain error ⁽³⁾ | V _{REF} = 1.5 V | 2.2 V | | | ±3.50 | % FSR |
| | | V _{REF} = 2.5 V | 3 V | | | | |
| d _{E(G)/dT} | Gain temperature coefficient ⁽³⁾ | | 2.2 V, 3 V | | 10 | | ppm of FSR/°C |
| t _{Offset_Cal} | Time for offset calibration ⁽⁴⁾ | DAC12AMPx = 2 | 2.2 V, 3 V | | | 100 | ms |
| | | DAC12AMPx = 3, 5 | | | | 32 | |
| | | DAC12AMPx = 4, 6, 7 | | | | 6 | |

- (1) Parameters calculated from the best-fit curve from 0x0A to 0xFFF. The best-fit curve method is used to deliver coefficients "a" and "b" of the first-order equation: $y = a + b \times x$. $V_{DAC12_xOUT} = E_O + (1 + E_G) \times (V_{eREF+}/4095) \times DAC12_xDAT$, DAC12IR = 1.
- (2) The offset calibration works on the output operational amplifier. Offset calibration is triggered setting bit DAC12CALON.
- (3) Parameters calculated from the best-fit curve from 0x0A to 0xFFF. The best-fit curve method is used to deliver coefficients "a" and "b" of the first-order equation: $y = a + b \times x$. $V_{DAC12_xOUT} = E_O + (1 + E_G) \times (V_{eREF+}/4095) \times DAC12_xDAT$, DAC12IR = 1.
- (4) The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx = {0, 1}. The DAC12 module should be configured prior to initiating calibration. Port activity during calibration may affect accuracy and is not recommended.

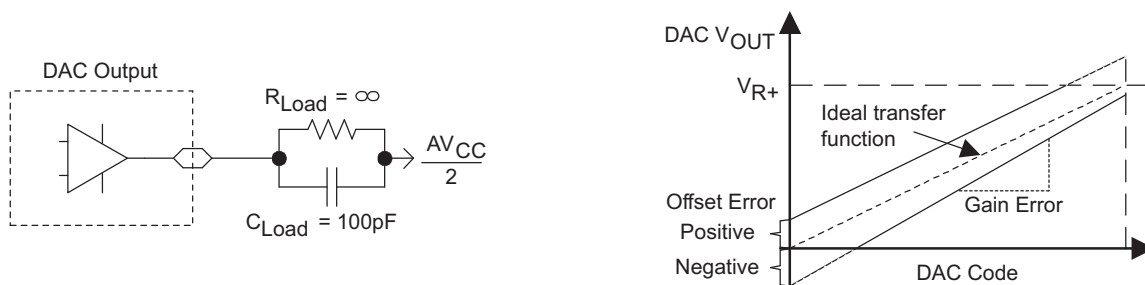


Figure 41. Linearity Test Load Conditions and Gain/Offset Definition

Typical Characteristics - 12-Bit DAC, Linearity Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

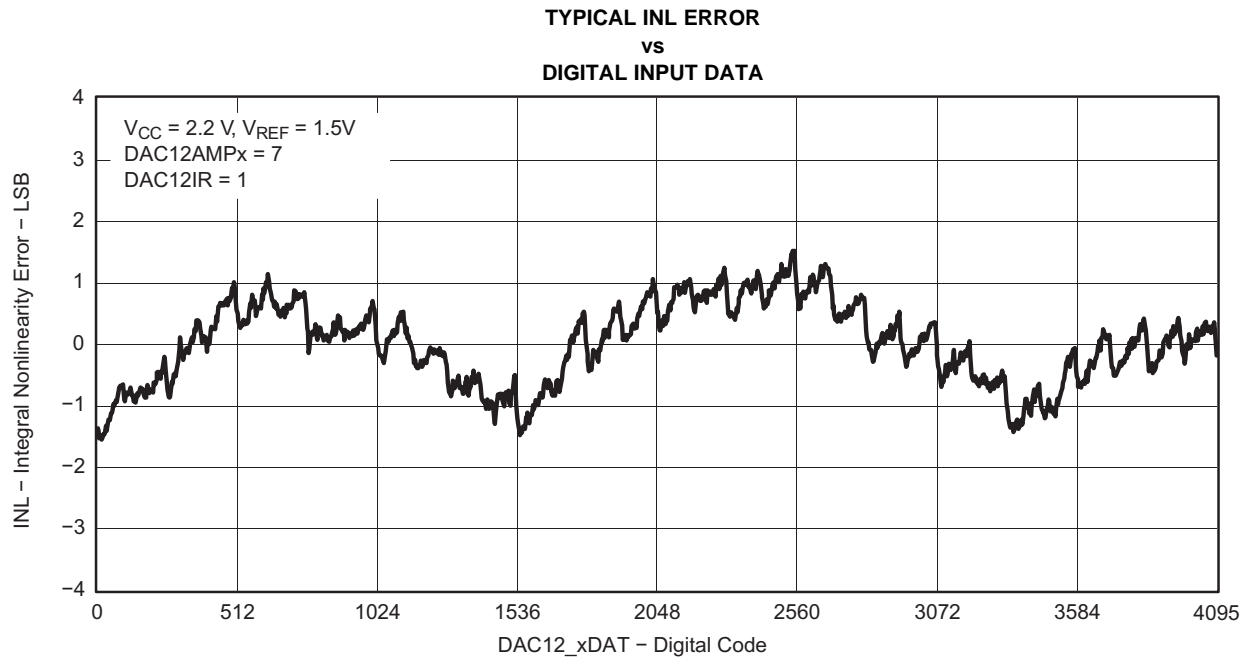


Figure 42.

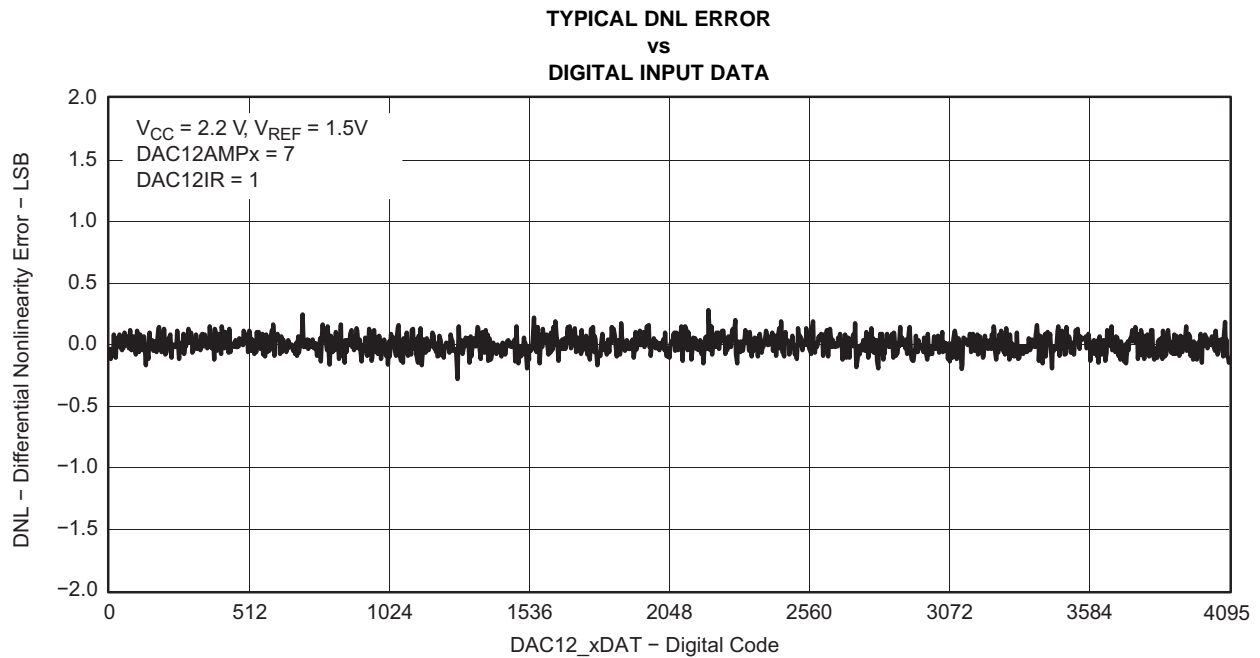


Figure 43.

12-Bit DAC Output Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | | |
|-------------------------|---|-----------------|--|-----|------------------|------|---|-----|
| V _O | No Load, V _{eREF+} = AV _{CC} , DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7 | 2.2 V, 3 V | 0 | | 0.005 | V | | |
| | No Load, V _{eREF+} = AV _{CC} , DAC12_xDAT = 0FFh, DAC12IR = 1, DAC12AMPx = 7 | | AV _{CC} - 0.05 | | AV _{CC} | | | |
| | R _{Load} = 3 kΩ, V _{eREF+} = AV _{CC} , DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7 | | 0 | | 0.1 | | | |
| | R _{Load} = 3 kΩ, V _{eREF+} = AV _{CC} , DAC12_xDAT = 0FFh, DAC12IR = 1, DAC12AMPx = 7 | | AV _{CC} - 0.13 | | AV _{CC} | | | |
| C _{L(DAC12)} | Maximum DAC12 load capacitance | 2.2 V, 3 V | | | 100 | pF | | |
| I _{L(DAC12)} | Maximum DAC12 load current | 2.2 V | -0.5 | | 0.5 | mA | | |
| | | 3 V | -1 | | 1 | | | |
| R _{O/P(DAC12)} | Output resistance (see Figure 44) | 2.2 V, 3 V | | | 150 | 250 | Ω | |
| | | | R _{Load} = 3 kΩ, V _{O/P(DAC12)} = 0 V, DAC12AMPx = 7, DAC12_xDAT = 0h | | | 150 | | 250 |
| | | | R _{Load} = 3 kΩ, V _{O/P(DAC12)} = AV _{CC} , DAC12AMPx = 7, DAC12_xDAT = 0FFh | | | 1 | | 4 |

(1) Data is valid after the offset calibration of the output amplifier.

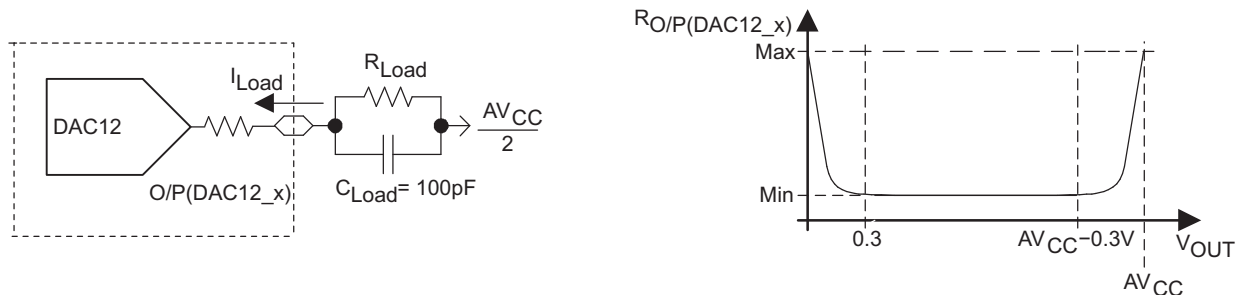


Figure 44. DAC12_x Output Resistance Tests

12-Bit DAC Reference Input Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---|--|-----------------|----------------------|-----|------------------------|------|
| V _{eREF+} | DAC12IR = 0 ⁽¹⁾⁽²⁾ | 2.2 V, 3 V | AV _{CC} / 3 | | AV _{CC} + 0.2 | V |
| | DAC12IR = 1 ⁽³⁾⁽⁴⁾ | | AV _{CC} | | AV _{CC} + 0.2 | |
| R _{i(VREF+)} , R _{i(VeREF+)} | DAC12_0 IR = DAC12_1 IR = 0 | 2.2 V, 3 V | 20 | | | MΩ |
| | DAC12_0 IR = 1, DAC12_1 IR = 0 | | 40 | 48 | 56 | kΩ |
| | DAC12_0 IR = 0, DAC12_1 IR = 1 | | 40 | 48 | 56 | |
| | DAC12_0 IR = DAC12_1 IR = 1, DAC12_0 SREFx = DAC12_1 SREFx ⁽⁵⁾ | | 20 | 24 | 28 | |

(1) For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AV_{CC}).

(2) The maximum voltage applied at reference input voltage terminal V_{eREF+} = [AV_{CC} - V_{E(O)}] / [3 × (1 + E_G)].

(3) For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AV_{CC}).

(4) The maximum voltage applied at reference input voltage terminal V_{eREF+} = [AV_{CC} - V_{E(O)}] / (1 + E_G).

(5) When DAC12IR = 1 and DAC12SREFx = 0 or 1 for both channels, the reference input resistive dividers for each DAC are in parallel reducing the reference input resistance.

12-Bit DAC Dynamic Specifications

$V_{REF} = V_{CC}$, DAC12IR = 1 (see Figure 45 and Figure 46), over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT | |
|--------------------|--|---|---------------------------|---|------------------------|---|---------------------|-----|
| t_{ON} | DAC12 on-time | DAC12_xDAT = 800h, Error $_{V(O)}$ < ± 0.5 LSB ⁽¹⁾ (see Figure 45) | DAC12AMPx = 0 → {2, 3, 4} | 2.2 V, 3 V | 60 | 120 | μ s | |
| | | | | | DAC12AMPx = 0 → {5, 6} | 15 | | 30 |
| | | | | | | DAC12AMPx = 0 → 7 | | 6 |
| $t_{S(FS)}$ | Settling time, full scale | DAC12_xDAT = 80h → F7Fh → 80h | DAC12AMPx = 2 | 2.2 V, 3 V | 100 | 200 | μ s | |
| | | | | | DAC12AMPx = 3, 5 | 40 | | 80 |
| | | | | | | DAC12AMPx = 4, 6, 7 | | 15 |
| $t_{S(C-C)}$ | Settling time, code to code | DAC12_xDAT = 3F8h → 408h → 3F8h BF8h → C08h → BF8h | DAC12AMPx = 2 | 2.2 V, 3 V | 5 | μ s | | |
| | | | | | DAC12AMPx = 3, 5 | | 2 | |
| | | | | | | | DAC12AMPx = 4, 6, 7 | 1 |
| SR | Slew rate ⁽²⁾ | DAC12_xDAT = 80h → F7Fh → 80h | DAC12AMPx = 2 | 2.2 V, 3 V | 0.05 | 0.12 | V/ μ s | |
| | | | | | DAC12AMPx = 3, 5 | 0.35 | | 0.7 |
| | | | | | | DAC12AMPx = 4, 6, 7 | | 1.5 |
| | Glitch energy, full scale | DAC12_xDAT = 80h → F7Fh → 80h | DAC12AMPx = 2 | 2.2 V, 3 V | 600 | nV-s | | |
| | | | | | DAC12AMPx = 3, 5 | | 150 | |
| | | | | | | | DAC12AMPx = 4, 6, 7 | 30 |
| BW _{-3dB} | 3-dB bandwidth, $V_{DC} = 1.5$ V, $V_{AC} = 0.1$ V _{PP} (see Figure 47) | DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h | 2.2 V, 3 V | 40 | kHz | | | |
| | | | | DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h | | 180 | | |
| | | | | | | DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h | 550 | |
| | Channel-to-channel crosstalk ⁽¹⁾ (see Figure 48) | DAC12_0DAT = 800h, No load, DAC12_1DAT = 80h ↔ F7Fh, $R_{Load} = 3$ k Ω , $f_{DAC12_1OUT} = 10$ kHz, Duty cycle = 50% | 2.2 V, 3 V | -80 | dB | | | |
| | | | | DAC12_0DAT = 80h ↔ F7Fh, $R_{Load} = 3$ k Ω , DAC12_1DAT = 800h, No load, $f_{DAC12_0OUT} = 10$ kHz, Duty cycle = 50% | | -80 | | |

(1) R_{Load} and C_{Load} are connected to AV_{SS} (not $AV_{CC}/2$) in Figure 45.

(2) Slew rate applies to output voltage steps ≥ 200 mV.

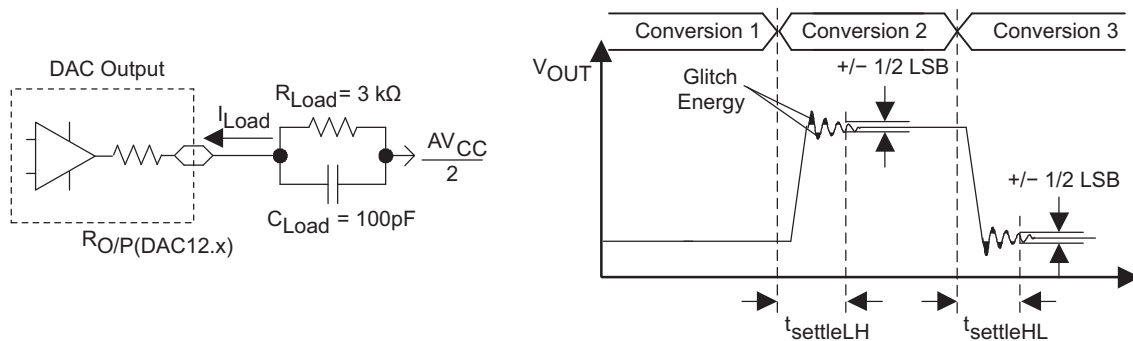


Figure 45. Settling Time and Glitch Energy Testing

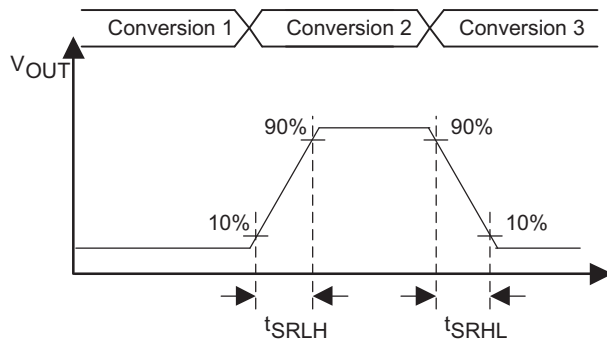


Figure 46. Slew Rate Testing

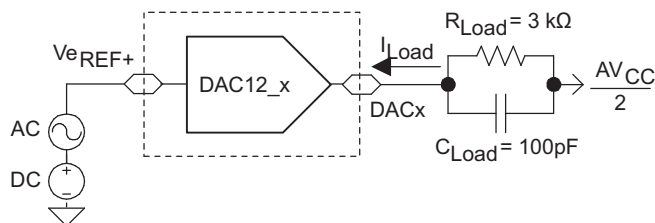


Figure 47. Test Conditions for 3-dB Bandwidth Specification

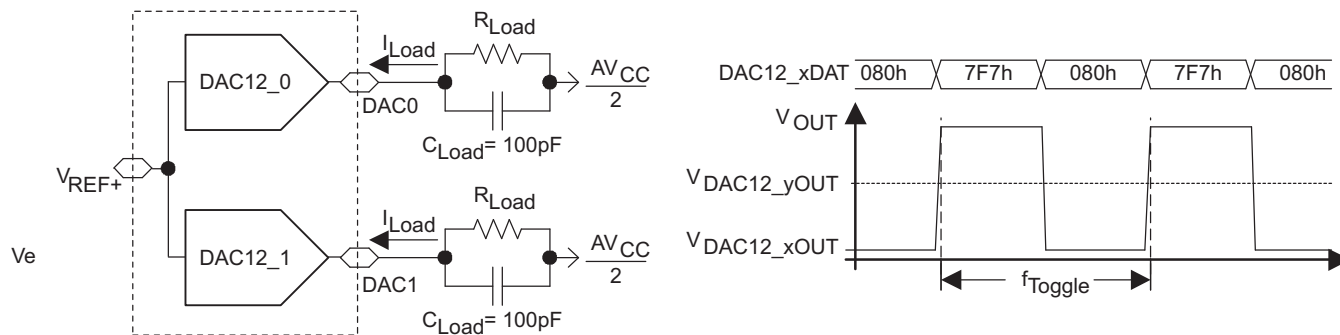


Figure 48. Crosstalk Test Conditions

Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------------------|---|-----------------------|-----------------|-----------------|-----------------|-----|------------------|
| V _{CC(PGM/ERASE)} | Program and erase supply voltage | | | 2.2 | | 3.6 | V |
| f _{FTG} | Flash timing generator frequency | | | 257 | | 476 | kHz |
| I _{PGM} | Supply current from V _{CC} during program | | 2.2 V/3.6 V | | 1 | 5 | mA |
| I _{ERASE} | Supply current from V _{CC} during erase | | 2.2 V/3.6 V | | 1 | 7 | mA |
| t _{CPT} | Cumulative program time ⁽¹⁾ | | 2.2 V/3.6 V | | | 10 | ms |
| t _{CMErase} | Cumulative mass erase time | | 2.2 V/3.6 V | 20 | | | ms |
| | Program and erase endurance | | | 10 ⁴ | 10 ⁵ | | cycles |
| t _{Retention} | Data retention duration | T _J = 25°C | | 100 | | | years |
| t _{Word} | Word or byte program time | ⁽²⁾ | | | 30 | | t _{FTG} |
| t _{Block, 0} | Block program time for first byte or word | ⁽²⁾ | | | 25 | | t _{FTG} |
| t _{Block, 1-63} | Block program time for each additional byte or word | ⁽²⁾ | | | 18 | | t _{FTG} |
| t _{Block, End} | Block program end-sequence wait time | ⁽²⁾ | | | 6 | | t _{FTG} |
| t _{Mass Erase} | Mass erase time | ⁽²⁾ | | | 10593 | | t _{FTG} |
| t _{Seg Erase} | Segment erase time | ⁽²⁾ | | | 4819 | | t _{FTG} |

- (1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
 (2) These values are hardwired into the Flash Controller's state machine (t_{FTG} = 1/f_{FTG}).

RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---------------------|---|-----------------|-----|-----|------|
| V _(RAMh) | RAM retention supply voltage ⁽¹⁾ | CPU halted | 1.6 | | V |

- (1) This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

JTAG Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|---|-----------------|-----|-----|-----|------|
| f _{TCK} | TCK input frequency ⁽¹⁾ | 2.2 V | 0 | | 5 | MHz |
| | | 3 V | 0 | | 10 | |
| R _{Internal} | Internal pullup resistance on TMS, TCK, and TDI/TCLK ⁽²⁾ | 2.2 V, 3 V | 25 | 60 | 90 | kΩ |

- (1) f_{TCK} may be restricted to meet the timing requirements of the module selected.
 (2) TMS, TCK, and TDI/TCLK pullup resistors are implemented in all versions.

JTAG Fuse⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---------------------|---|-----------------------|-----|-----|------|
| V _{CC(FB)} | Supply voltage during fuse-blow condition | T _A = 25°C | 2.5 | | V |
| V _{FB} | Voltage level on TEST for fuse blow | | 6 | 7 | V |
| I _{FB} | Supply current into TEST during fuse blow | | | 100 | mA |
| t _{FB} | Time to blow fuse | | | 1 | ms |

- (1) Once the fuse is blown, no further access to the JTAG/Test and emulation feature is possible, and JTAG is switched to bypass mode.

APPLICATION INFORMATION

Port P1 (P1.0 to P1.7), Input/Output With Schmitt Trigger

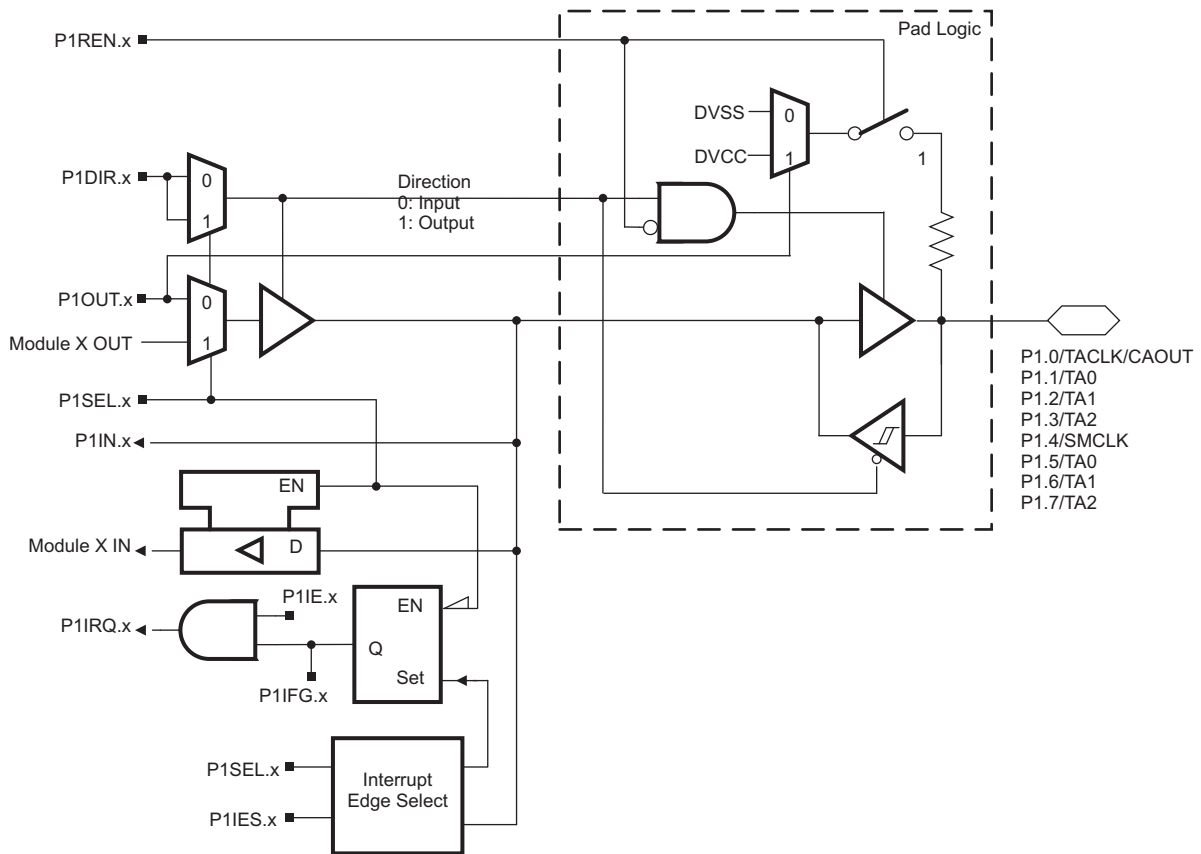


Table 15. Port P1 (P1.0 to P1.7) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS / SIGNALS | |
|------------------|---|----------------|------------------------|---------|
| | | | P1DIR.x | P1SEL.x |
| P1.0/TACLK/CAOUT | 0 | P1.0 (I/O) | I: 0; O: 1 | 0 |
| | | Timer_A3.TACLK | 0 | 1 |
| | | CAOUT | 1 | 1 |
| P1.1/TA0 | 1 | P1.1 (I/O) | I: 0; O: 1 | 0 |
| | | Timer_A3.CCI0A | 0 | 1 |
| | | Timer_A3.TA0 | 1 | 1 |
| P1.2/TA1 | 2 | P1.2 (I/O) | I: 0; O: 1 | 0 |
| | | Timer_A3.CCI1A | 0 | 1 |
| | | Timer_A3.TA1 | 1 | 1 |
| P1.3/TA2 | 3 | P1.3 (I/O) | I: 0; O: 1 | 0 |
| | | Timer_A3.CCI2A | 0 | 1 |
| | | Timer_A3.TA2 | 1 | 1 |
| P1.4/SMCLK | 4 | P1.4 (I/O) | I: 0; O: 1 | 0 |
| | | SMCLK | 1 | 1 |
| P1.5/TA0 | 5 | P1.5 (I/O) | I: 0; O: 1 | 0 |
| | | Timer_A3.TA0 | 1 | 1 |
| P1.6/TA1 | 6 | P1.6 (I/O) | I: 0; O: 1 | 0 |
| | | Timer_A3.TA1 | 1 | 1 |
| P1.7/TA2 | 7 | P1.7 (I/O) | I: 0; O: 1 | 0 |
| | | Timer_A3.TA2 | 1 | 1 |

Port P2 (P2.0 to P2.4, P2.6, and P2.7), Input/Output With Schmitt Trigger

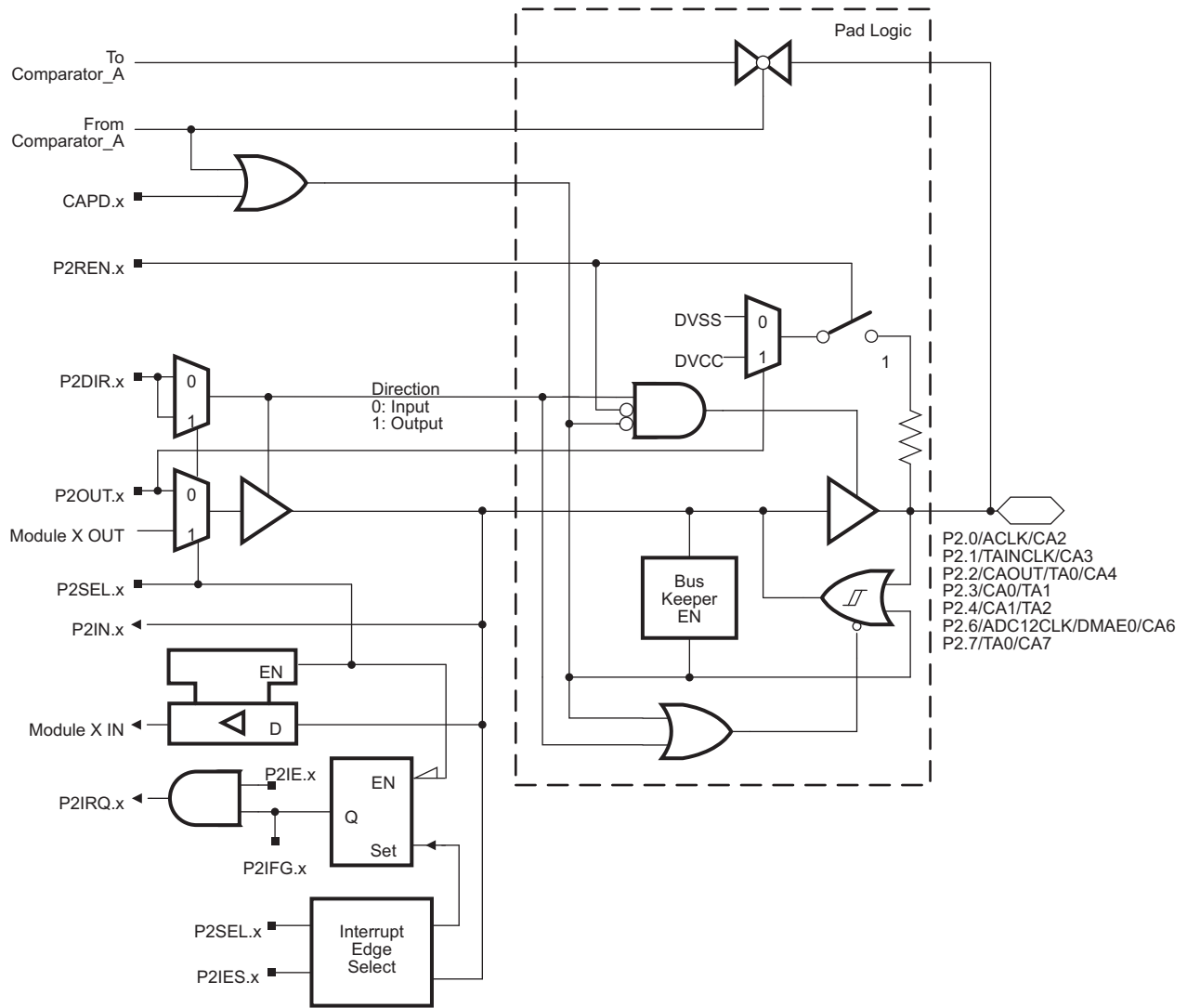


Table 16. Port P2 (P2.0 to P2.4, P2.6, and P2.7) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS / SIGNALS ⁽¹⁾ | | |
|---|---|------------------|---------------------------------------|------------|---------|
| | | | CAPD.x | P2DIR.x | P2SEL.x |
| P2.0/ACLK/CA2 | 0 | P2.0 (I/O) | 0 | I: 0; O: 1 | 0 |
| | | ACLK | 0 | 1 | 1 |
| | | CA2 | 1 | X | X |
| P2.1/TAINCLK/CA3 | 1 | P2.1 (I/O) | 0 | I: 0; O: 1 | 0 |
| | | Timer_A3.INCLK | 0 | 0 | 1 |
| | | DV _{SS} | 0 | 1 | 1 |
| | | CA3 | 1 | X | X |
| P2.2/CAOUT/TA0/CA4 | 2 | P2.2 (I/O) | 0 | I: 0; O: 1 | 0 |
| | | CAOUT | 0 | 1 | 1 |
| | | Timer_A3.CCI0B | 0 | 0 | 1 |
| | | CA4 | 1 | X | X |
| P2.3/CA0/TA1 | 3 | P2.3 (I/O) | 0 | I: 0; O: 1 | 0 |
| | | Timer_A3.TA1 | 0 | 1 | 1 |
| | | CA0 | 1 | X | X |
| P2.4/CA1/TA2 | 4 | P2.4 (I/O) | 0 | I: 0; O: 1 | 0 |
| | | Timer_A3.TA2 | 0 | 1 | X |
| | | CA1 | 1 | X | 1 |
| P2.6/ADC12CLK/ DMAE0 ⁽²⁾ /CA6 | 6 | P2.6 (I/O) | 0 | I: 0; O: 1 | 0 |
| | | ADC12CLK | 0 | 1 | 1 |
| | | DMAE0 | 0 | 0 | 1 |
| | | CA6 | 1 | X | X |
| P2.7/TA0/CA7 | 7 | P2.7 (I/O) | 0 | I: 0; O: 1 | 0 |
| | | Timer_A3.TA0 | 0 | 1 | 1 |
| | | CA7 | 1 | X | X |

- (1) X = Don't care
- (2) MSP430F261x devices only

Port P2 (P2.5), Input/Output With Schmitt Trigger

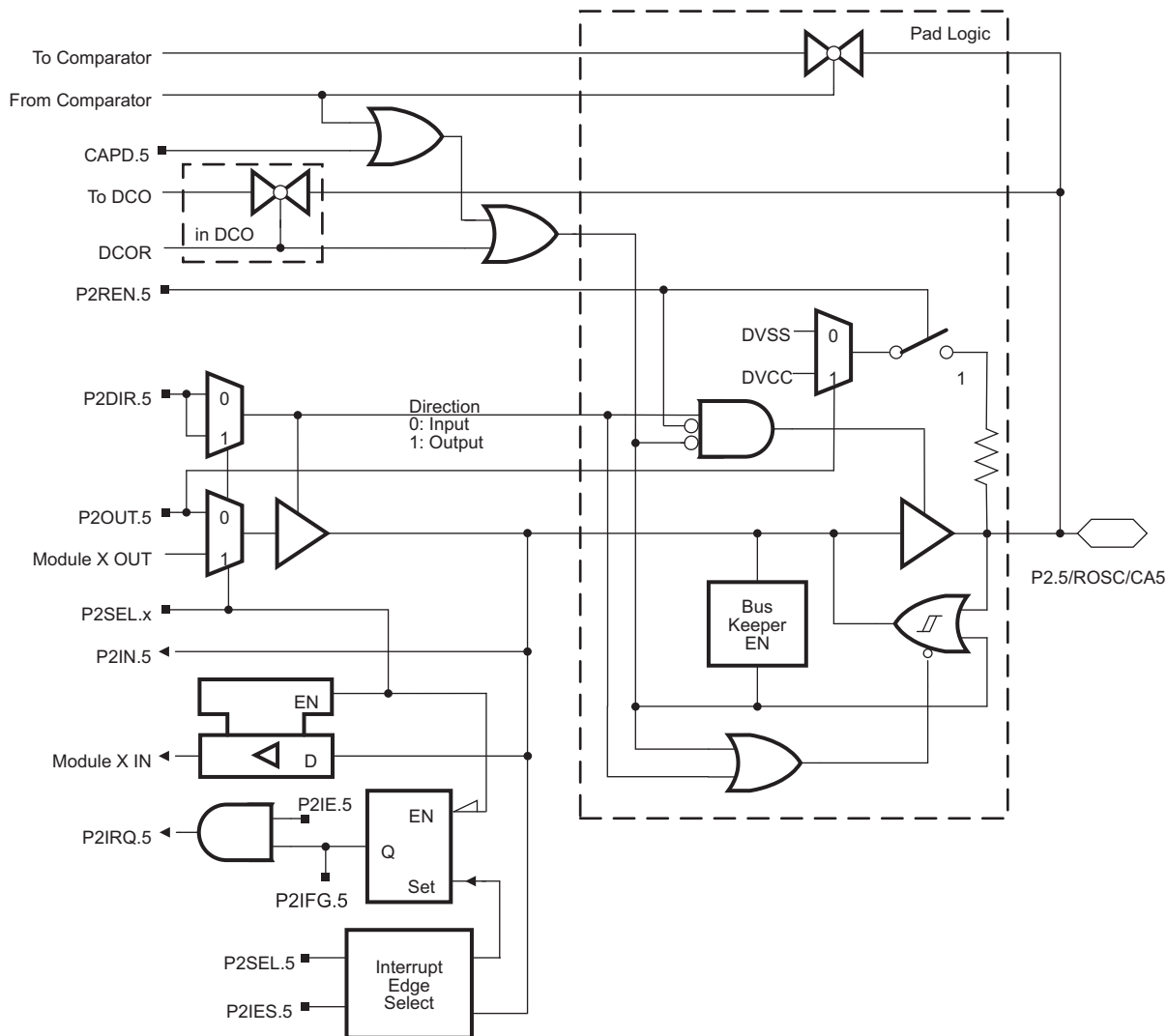


Table 17. Port P2 (P2.5) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS / SIGNALS ⁽¹⁾ | | | |
|----------------------------|---|---------------------------------|---------------------------------------|------|------------|---------|
| | | | CAPD | DCOR | P2DIR.5 | P2SEL.5 |
| P2.5/R _{OSC} /CA5 | 5 | P2.5 (I/O) | 0 | 0 | I: 0; O: 1 | 0 |
| | | R _{OSC} ⁽²⁾ | 0 | 1 | X | X |
| | | DV _{SS} | 0 | 0 | 1 | 1 |
| | | CA5 | 1 or selected | 0 | X | X |

(1) X = Don't care

(2) If R_{OSC} is used, it is connected to an external resistor.

Port P3 (P3.0 to P3.7), Input/Output With Schmitt Trigger

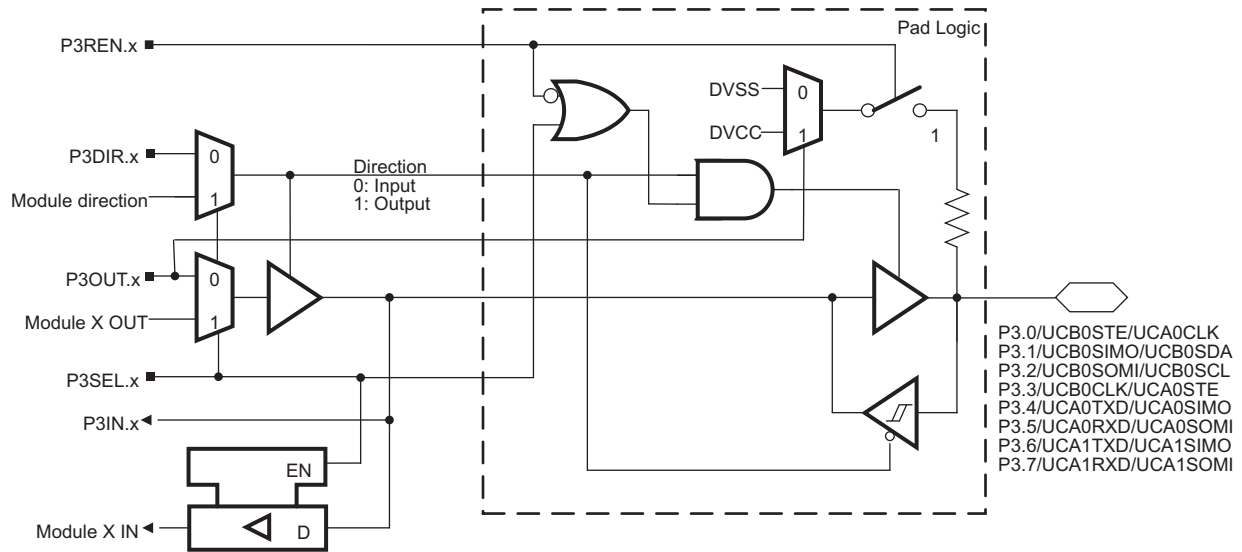


Table 18. Port P3 (P3.0 to P3.7) Pin Functions

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS / SIGNALS ⁽¹⁾ | |
|---------------------------|---|------------------------------------|---------------------------------------|---------|
| | | | P3DIR.x | P3SEL.x |
| P3.0/UCB0STE/ UCA0CLK | 0 | P3.0 (I/O) | I: 0; O: 1 | 0 |
| | | UCB0STE/UCA0CLK ⁽²⁾⁽³⁾ | X | 1 |
| P3.1/UCB0SIMO/ UCB0SDA | 1 | P3.1 (I/O) | I: 0; O: 1 | 0 |
| | | UCB0SIMO/UCB0SDA ⁽⁴⁾⁽⁵⁾ | X | 1 |
| P3.2/UCB0SOMI/ UCB0SCL | 2 | P3.2 (I/O) | I: 0; O: 1 | 0 |
| | | UCB0SOMI/UCB0SCL ⁽⁴⁾⁽⁵⁾ | X | 1 |
| P3.3/UCB0CLK/ UCA0STE | 3 | P3.3 (I/O) | I: 0; O: 1 | 0 |
| | | UCB0CLK/UCA0STE ⁽⁴⁾ | X | 1 |
| P3.4/UCA0TXD/ UCA0SIMO | 4 | P3.4 (I/O) | I: 0; O: 1 | 0 |
| | | UCA0TXD/UCA0SIMO ⁽⁴⁾ | X | 1 |
| P3.5/UCA0RXD/ UCA0SOMI | 5 | P3.5 (I/O) | I: 0; O: 1 | 0 |
| | | UCA0RXD/UCA0SOMI ⁽⁴⁾ | X | 1 |
| P3.6/UCA1TXD/ UCA1SIMO | 6 | P3.6 (I/O) | I: 0; O: 1 | 0 |
| | | UCA1TXD/UCA1SIMO ⁽⁴⁾ | X | 1 |
| P3.7/UCA1RXD/ UCA1SOMI | 7 | P3.7 (I/O) | I: 0; O: 1 | 0 |
| | | UCA1RXD/UCA1SOMI ⁽⁴⁾ | X | 1 |

(1) X = Don't care

(2) The pin direction is controlled by the USCI module.

(3) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI_A0/B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

(4) The pin direction is controlled by the USCI module.

(5) If the I2C functionality is selected, the output drives only the logical 0 to V_{SS} level.

Port P4 (P4.0 to P4.7), Input/Output With Schmitt Trigger

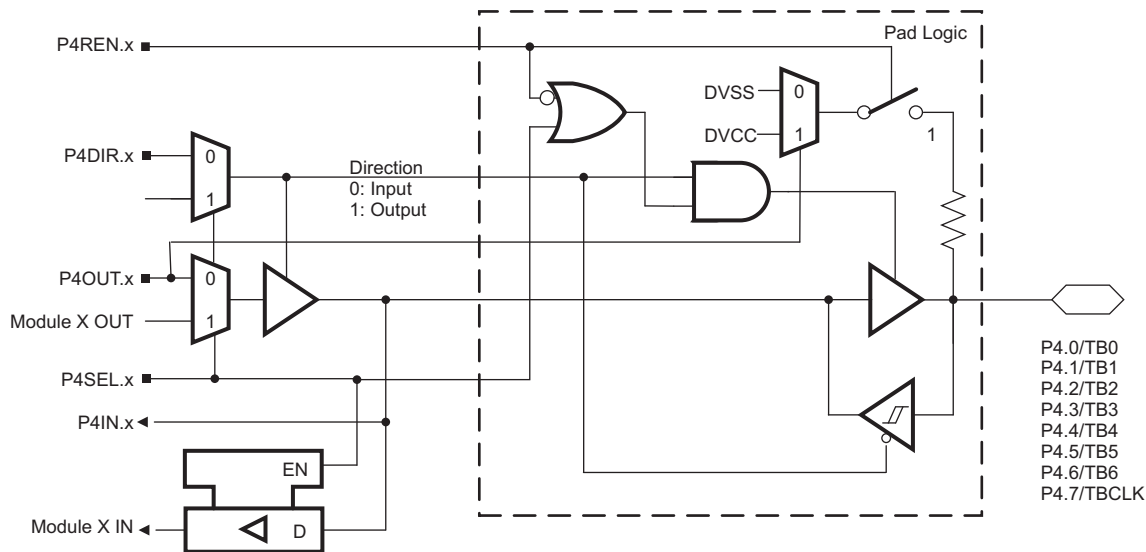


Table 19. Port P4 (P4.0 to P4.7) Pin Functions

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS / SIGNALS ⁽¹⁾ | |
|-----------------|---|-----------------------------------|---------------------------------------|---------|
| | | | P4DIR.x | P4SEL.x |
| P4.0/TB0 | 0 | P4.0 (I/O) | I: 0; O: 1 | 0 |
| | | Timer_B7.CCI0A and Timer_B7.CCI0B | 0 | 1 |
| | | Timer_B7.TB0 | 1 | 1 |
| P4.1/TB1 | 1 | P4.1 (I/O) | I: 0; O: 1 | 0 |
| | | Timer_B7.CCI1A and Timer_B7.CCI1B | 0 | 1 |
| | | Timer_B7.TB1 | 1 | 1 |
| P4.2/TB2 | 2 | P4.2 (I/O) | I: 0; O: 1 | 0 |
| | | Timer_B7.CCI2A and Timer_B7.CCI2B | 0 | 1 |
| | | Timer_B7.TB2 | 1 | 1 |
| P4.3/TB3 | 3 | P4.3 (I/O) | I: 0; O: 1 | 0 |
| | | Timer_B7.CCI3A and Timer_B7.CCI3B | 0 | 1 |
| | | Timer_B7.TB3 | 1 | 1 |
| P4.4/TB4 | 4 | P4.4 (I/O) | I: 0; O: 1 | 0 |
| | | Timer_B7.CCI4A and Timer_B7.CCI4B | 0 | 1 |
| | | Timer_B7.TB4 | 1 | 1 |
| P4.5/TB5 | 5 | P4.5 (I/O) | I: 0; O: 1 | 0 |
| | | Timer_B7.CCI5A and Timer_B7.CCI5B | 0 | 1 |
| | | Timer_B7.TB5 | 1 | 1 |
| P4.6/TB6 | 6 | P4.6 (I/O) | I: 0; O: 1 | 0 |
| | | Timer_B7.CCI6A and Timer_B7.CCI6B | 0 | 1 |
| | | Timer_B7.TB6 | 1 | 1 |
| P4.7/TBCLK | 7 | P4.7 (I/O) | I: 0; O: 1 | 0 |
| | | Timer_B7.TBCLK | 1 | 1 |

(1) X = Don't care

Port P5 (P5.0 to P5.7), Input/Output With Schmitt Trigger

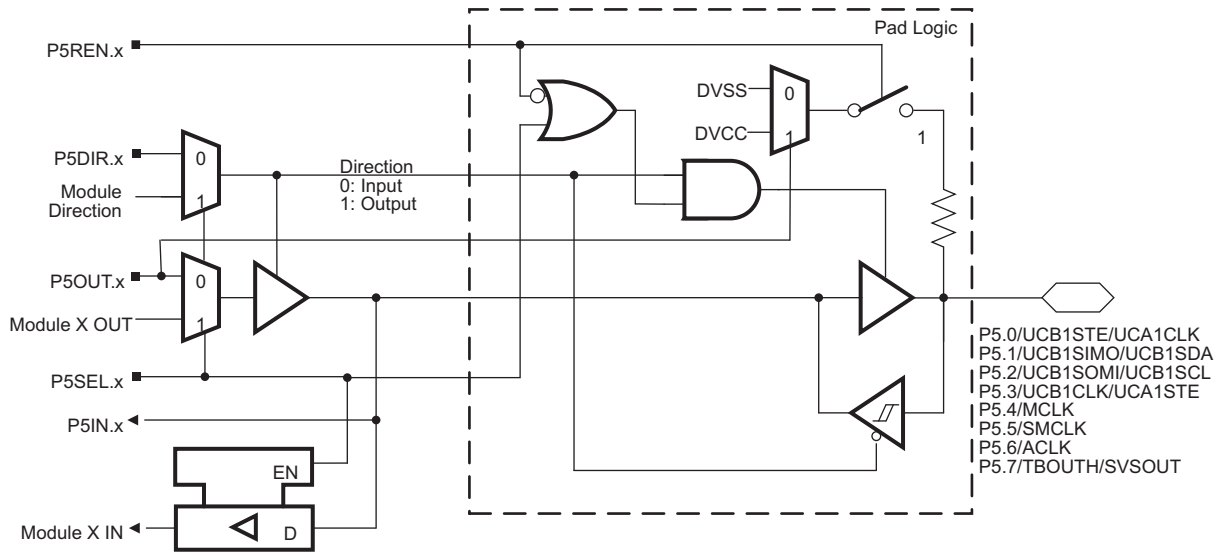


Table 20. Port P5 (P5.0 to P5.7) Pin Functions

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS / SIGNALS ⁽¹⁾ | |
|---------------------------|---|------------------------------------|---------------------------------------|---------|
| | | | P5DIR.x | P5SEL.x |
| P5.0/UCB1STE/ UCA1CLK | 0 | P5.0 (I/O) | I: 0; O: 1 | 0 |
| | | UCB1STE/UCA1CLK ⁽²⁾⁽³⁾ | X | 1 |
| P5.1/UCB1SIMO/ UCB1SDA | 1 | P5.1 (I/O) | I: 0; O: 1 | 0 |
| | | UCB1SIMO/UCB1SDA ⁽²⁾⁽⁴⁾ | X | 1 |
| P5.2/UCB1SOMI/ UCB1SCL | 2 | P5.2 (I/O) | I: 0; O: 1 | 0 |
| | | UCB1SOMI/UCB1SCL ⁽²⁾⁽⁴⁾ | X | 1 |
| P5.3/UCB1CLK/ UCA1STE | 3 | P5.3 (I/O) | I: 0; O: 1 | 0 |
| | | UCB1CLK/UCA1STE ⁽²⁾ | X | 1 |
| P5.4/MCLK | 4 | P5.0 (I/O) | I: 0; O: 1 | 0 |
| | | MCLK | 1 | 1 |
| P5.5/SMCLK | 5 | P5.1 (I/O) | I: 0; O: 1 | 0 |
| | | SMCLK | 1 | 1 |
| P5.6/ACLK | 6 | P5.2 (I/O) | I: 0; O: 1 | 0 |
| | | ACLK | 1 | 1 |
| P5.7/TBOUTH/SVSOUT | 7 | P5.7 (I/O) | I: 0; O: 1 | 0 |
| | | TBOUTH | 0 | 1 |
| | | SVSOUT | 1 | 1 |

(1) X = Don't care

(2) The pin direction is controlled by the USCI module.

(3) UCA1CLK function takes precedence over UCB1STE function. If the pin is required as UCA1CLK input or output USCI_A1/B1 will be forced to 3-wire SPI mode if 4-wire SPI mode is selected.

(4) If the I2C functionality is selected, the output drives only the logical 0 to V_{SS} level.

Port P6 (P6.0 to P6.4), Input/Output With Schmitt Trigger

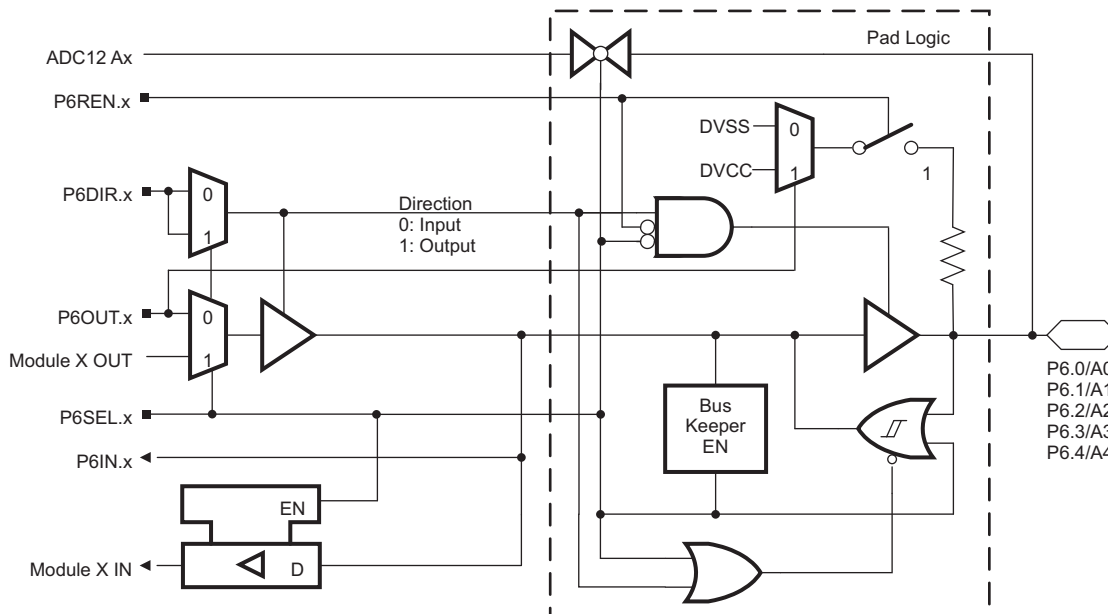


Table 21. Port P6 (P6.0 to P6.4) Pin Functions

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS / SIGNALS ⁽¹⁾ | | |
|-----------------|---|-------------------|---------------------------------------|---------|-----------|
| | | | P6DIR.x | P6SEL.x | INCH.x |
| P6.0/A0 | 0 | P6.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A0 ⁽²⁾ | X | 1 | 1 (y = 0) |
| P6.1/A1 | 1 | P6.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A1 ⁽²⁾ | X | 1 | 1 (y = 1) |
| P6.2/A2 | 2 | P6.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A2 ⁽²⁾ | X | 1 | 1 (y = 2) |
| P6.3/A3 | 3 | P6.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A3 ⁽²⁾ | X | 1 | 1 (y = 3) |
| P6.4/A4 | 4 | P6.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A4 ⁽²⁾ | X | 1 | 1 (y = 4) |

(1) X = Don't care

(2) The ADC12 channel Ax is connected to AV_{SS} internally if not selected.

Port P6 (P6.5 and P6.6), Input/Output With Schmitt Trigger

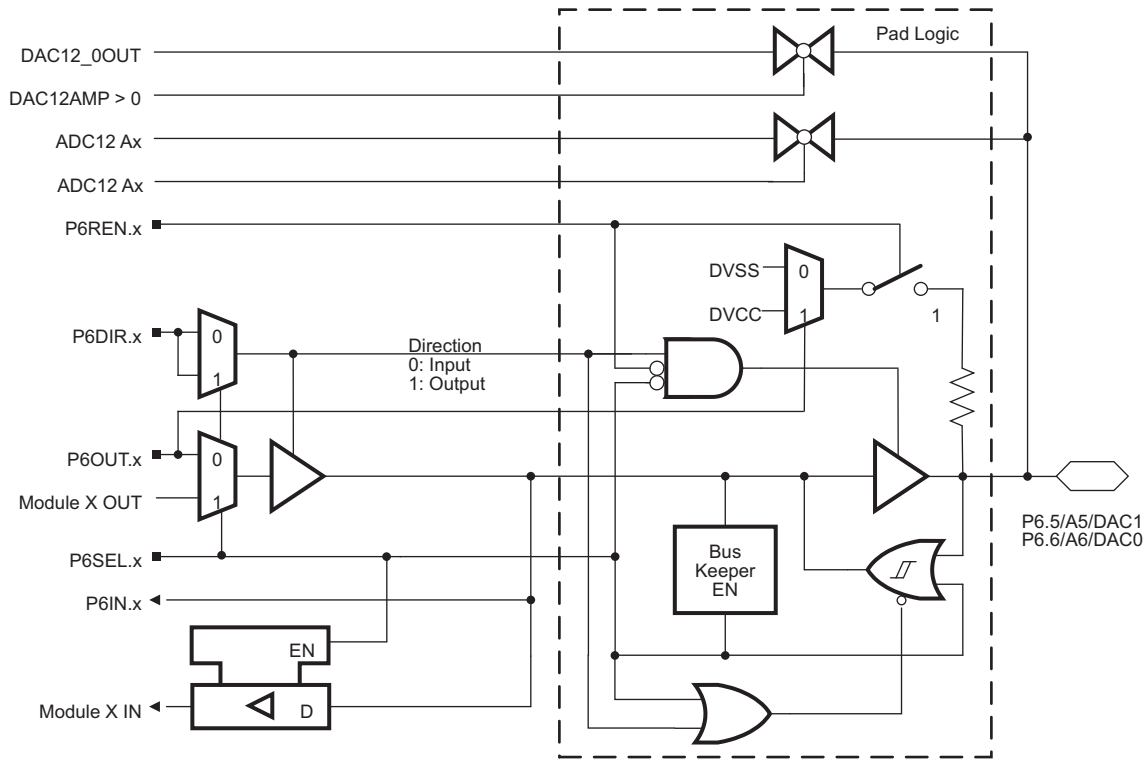


Table 22. Port P6 (P6.5 and P6.6) Pin Functions

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS / SIGNALS ⁽¹⁾ | | | |
|-----------------------------|---|------------------------------------|---------------------------------------|---------|--------------|-----------|
| | | | P6DIR.x | P6SEL.x | DAC12AMP > 0 | INCH.y |
| P6.5/A5/DAC1 ⁽²⁾ | 5 | P6.5 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | DV _{SS} | 1 | 1 | 0 | 0 |
| | | A5 ⁽³⁾ | X | X | 0 | 1 (y = 5) |
| | | DAC1 (DAC12OPS = 1) ⁽⁴⁾ | X | X | 1 | 0 |
| P6.6/A6/DAC0 ⁽⁵⁾ | 6 | P6.6 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | DV _{SS} | 1 | 1 | 0 | 0 |
| | | A6 ⁽⁶⁾ | X | X | 0 | 1 (y = 6) |
| | | DAC0 (DAC12OPS = 0) ⁽⁷⁾ | X | X | 1 | 0 |

- (1) X = Don't care
- (2) MSP430F261x devices only
- (3) The ADC12 channel Ax is connected to AV_{SS} internally if not selected.
- (4) The DAC outputs are floating if not selected.
- (5) MSP430F261x devices only
- (6) The ADC12 channel Ax is connected to AV_{SS} internally if not selected.
- (7) The DAC outputs are floating if not selected.

Port P6 (P6.7), Input/Output With Schmitt Trigger

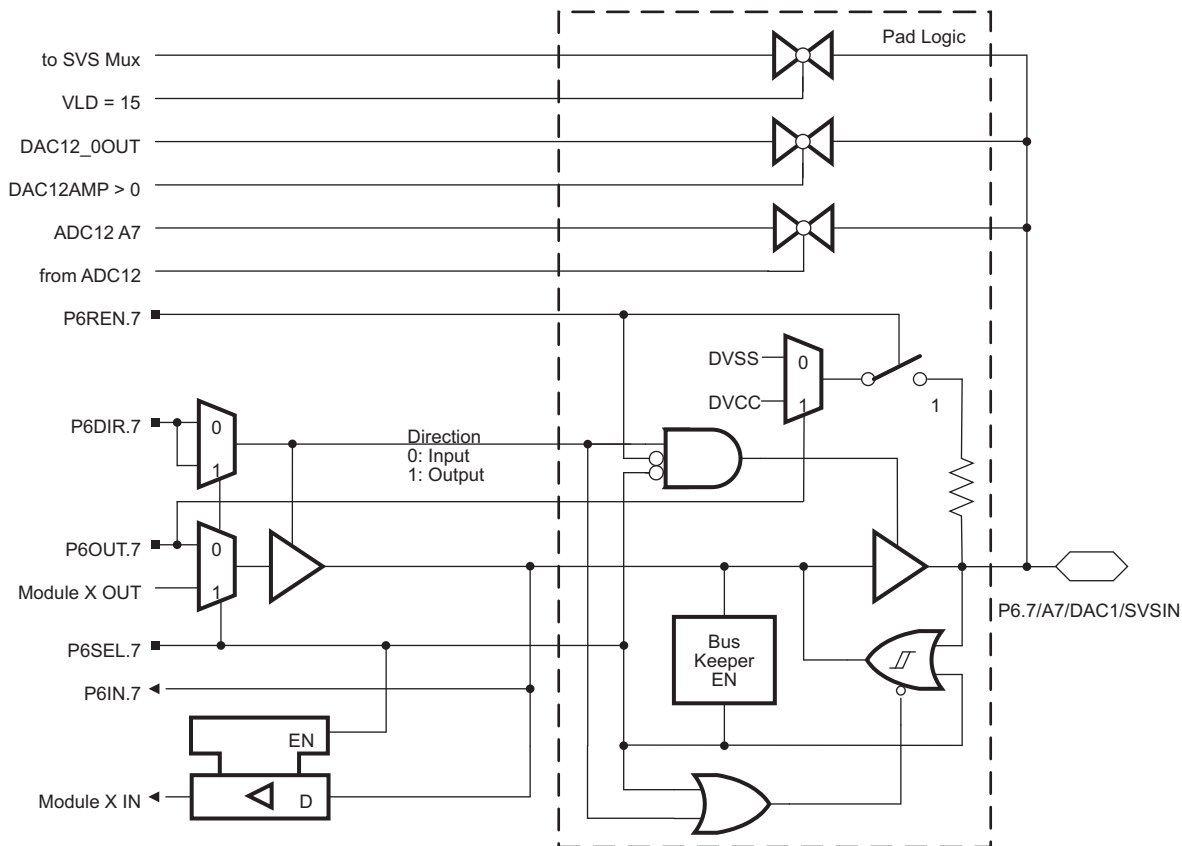


Table 23. Port P6 (P6.7) Pin Functions

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS / SIGNALS ⁽¹⁾ | | | |
|---|---|------------------------------------|---------------------------------------|---------|-----------|------------|
| | | | P6DIR.x | P6SEL.x | INCH.y | DAC12AMP>0 |
| P6.7/A7/DAC1 ⁽²⁾ / SVSIN ⁽²⁾ | 7 | P6.7 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | DV _{SS} | 1 | 1 | 0 | 0 |
| | | A7 ⁽³⁾ | X | 1 | 1 (y = 7) | 0 |
| | | DAC1 (DAC12OPS = 0) ⁽⁴⁾ | X | 1 | 0 | 1 |
| | | SVSIN (VLD = 15) | X | 1 | 0 | 0 |

- (1) X = Don't care
- (2) MSP430F261x devices only
- (3) The ADC12 channel Ax is connected to AV_{SS} internally if not selected.
- (4) The DAC outputs are floating if not selected.

Port P7 (P7.0 to P7.7), Input/Output With Schmitt Trigger⁽⁵⁾

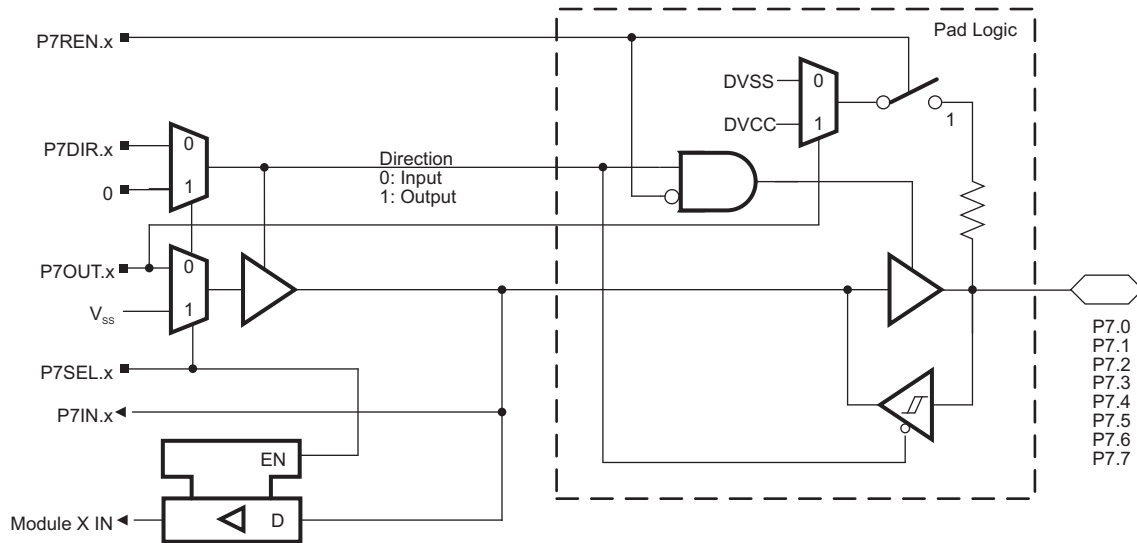


Table 24. Port P7 (P7.0 to P7.7) Pin Functions⁽¹⁾

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS / SIGNALS ⁽²⁾ | |
|-----------------|---|------------|---------------------------------------|---------|
| | | | P7DIR.x | P7SEL.x |
| P7.0 | 0 | P7.0 (I/O) | I: 0; O: 1 | 0 |
| | | Input | X | 1 |
| P7.1 | 1 | P7.1 (I/O) | I: 0; O: 1 | 0 |
| | | Input | X | 1 |
| P7.2 | 2 | P7.2 (I/O) | I: 0; O: 1 | 0 |
| | | Input | X | 1 |
| P7.3 | 3 | P7.3 (I/O) | I: 0; O: 1 | 0 |
| | | Input | X | 1 |
| P7.4 | 4 | P7.4 (I/O) | I: 0; O: 1 | 0 |
| | | Input | X | 1 |
| P7.5 | 5 | P7.5 (I/O) | I: 0; O: 1 | 0 |
| | | Input | X | 1 |
| P7.6 | 6 | P7.6 (I/O) | I: 0; O: 1 | 0 |
| | | Input | X | 1 |
| P7.7 | 7 | P7.7 (I/O) | I: 0; O: 1 | 0 |
| | | Input | X | 1 |

(5) 80-pin devices only

(1) 80-pin devices only

(2) X = Don't care

Port P8 (P8.0 to P8.5), Input/Output With Schmitt Trigger⁽³⁾

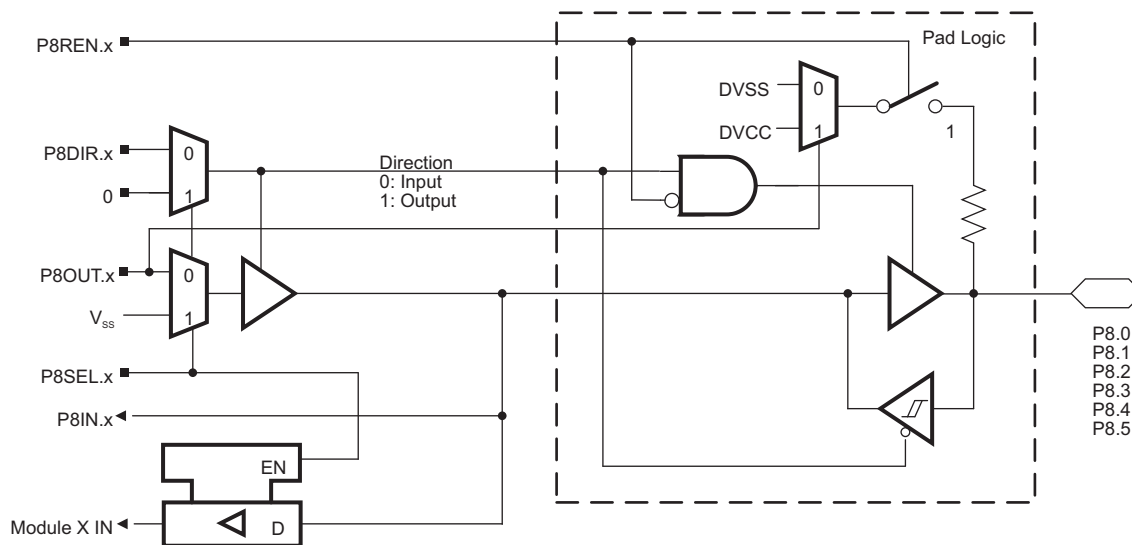


Table 25. Port P8 (P8.0 to P8.5) Pin Functions⁽¹⁾

| PIN NAME (P8.x) | x | FUNCTION | CONTROL BITS / SIGNALS ⁽²⁾ | |
|-----------------|---|------------|---------------------------------------|---------|
| | | | P8DIR.x | P8SEL.x |
| P8.0 | 0 | P8.0 (I/O) | I: 0; O: 1 | 0 |
| | | Input | X | 1 |
| P8.1 | 1 | P8.1 (I/O) | I: 0; O: 1 | 0 |
| | | Input | X | 1 |
| P8.2 | 2 | P8.2 (I/O) | I: 0; O: 1 | 0 |
| | | Input | X | 1 |
| P8.3 | 3 | P8.3 (I/O) | I: 0; O: 1 | 0 |
| | | Input | X | 1 |
| P8.4 | 4 | P8.4 (I/O) | I: 0; O: 1 | 0 |
| | | Input | X | 1 |
| P8.5 | 5 | P8.5 (I/O) | I: 0; O: 1 | 0 |
| | | Input | X | 1 |

(3) 80-pin devices only

(1) 80-pin devices only

(2) X = Don't care

Port P8 (P8.6), Input/Output With Schmitt Trigger⁽³⁾

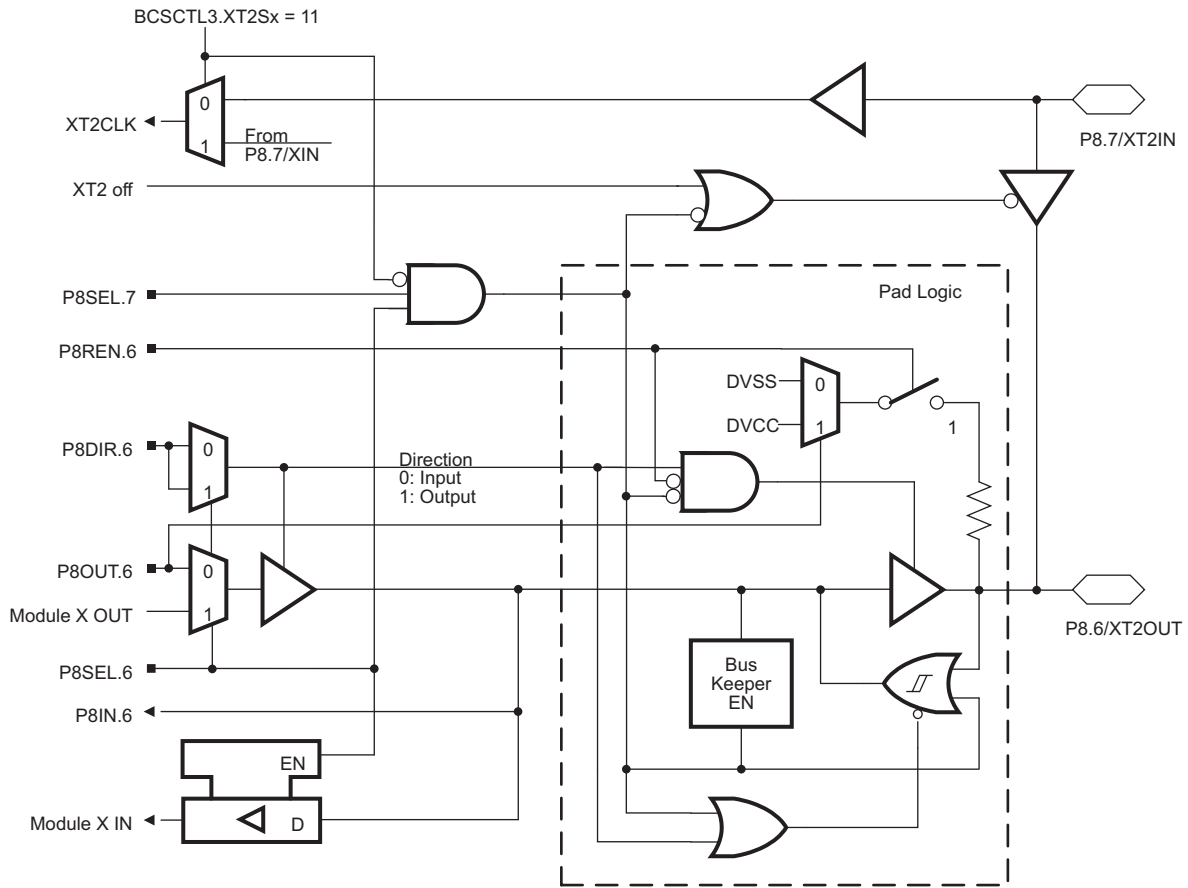


Table 26. Port P8 (P8.6) Pin Functions⁽¹⁾

| PIN NAME (P8.x) | x | FUNCTION | CONTROL BITS / SIGNALS | |
|-----------------|---|------------------|------------------------|---------|
| | | | P8DIR.x | P8SEL.x |
| P8.6/XT2OUT | 6 | P8.6 (I/O) | I: 0; O: 1 | 0 |
| | | XT2OUT (default) | 0 | 1 |
| | | DV _{SS} | 1 | 1 |

(3) 80-pin devices only

(1) 80-pin devices only

Port P8 (P8.7), Input/Output With Schmitt Trigger⁽²⁾

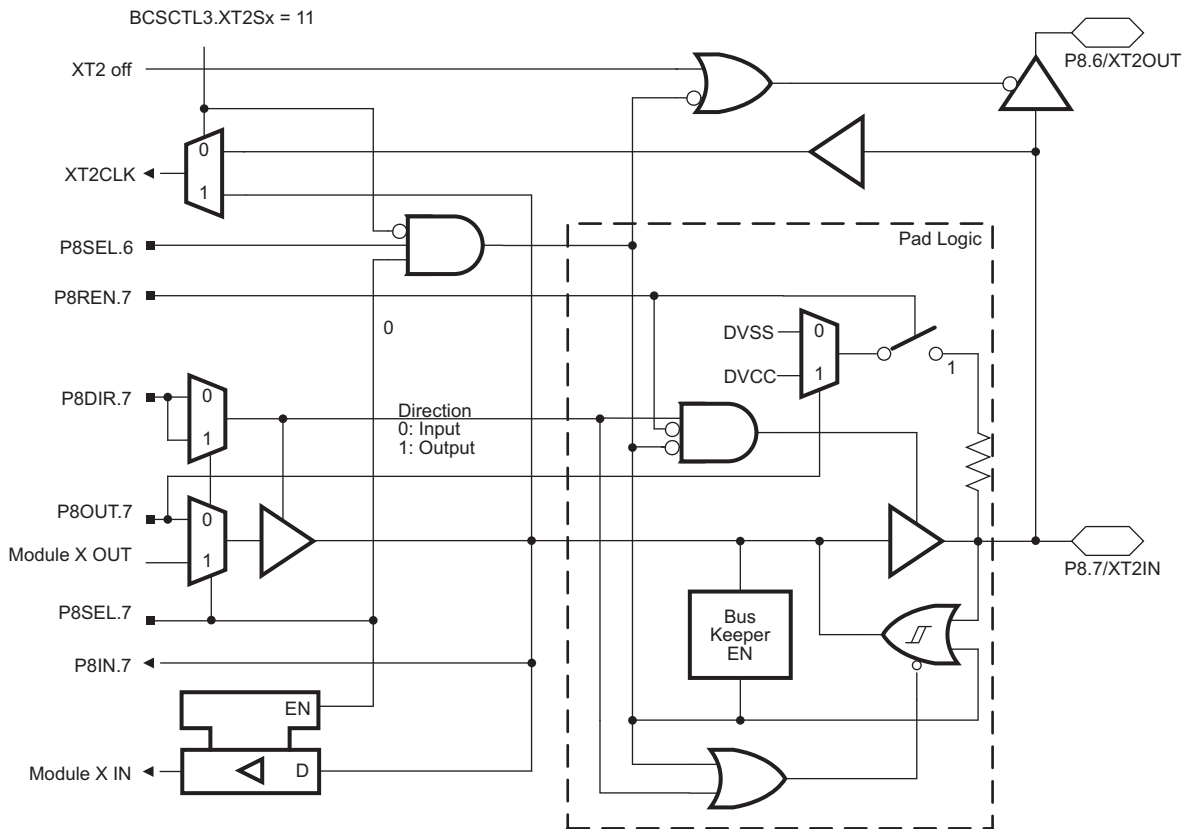


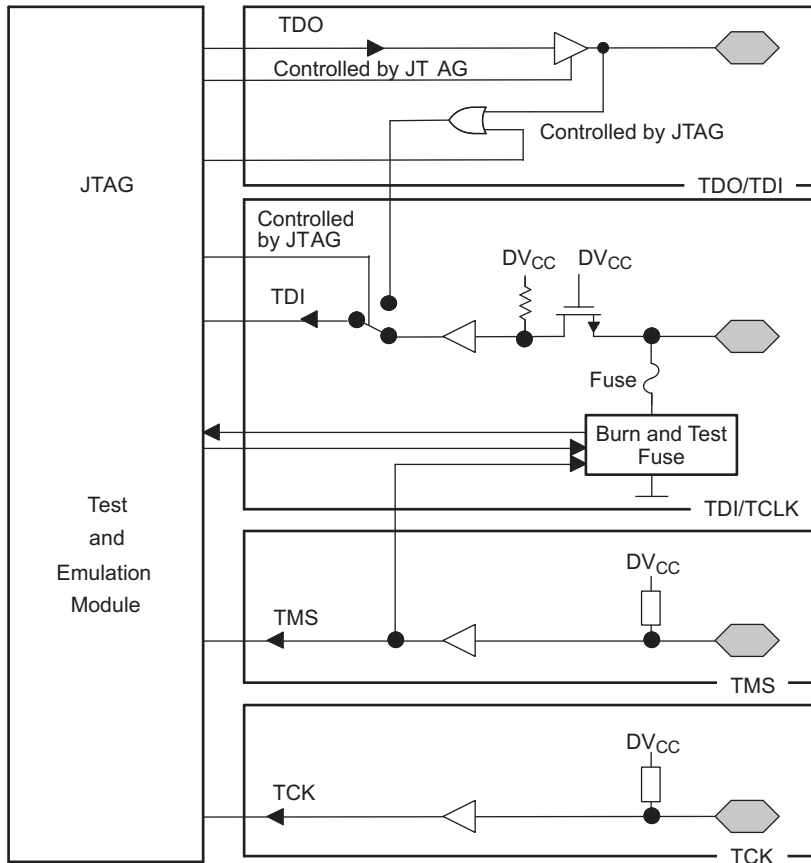
Table 27. Port P8 (P8.7) Pin Functions⁽¹⁾

| PIN NAME (P8.x) | x | FUNCTION | CONTROL BITS / SIGNALS | |
|-----------------|---|-----------------|------------------------|---------|
| | | | P8DIR.x | P8SEL.x |
| P8.7/XT2IN | 7 | P8.7 (I/O) | I: 0; O: 1 | 0 |
| | | XT2IN (default) | 0 | 1 |
| | | V _{SS} | 1 | 1 |

(2) 80-pin devices only

(1) 80-pin devices only

JTAG Pins: TMS, TCK, TDI/TCLK, TDO/TDI, Input/Output With Schmitt Trigger



During Programming Activity and During Blowing of the Fuse, Pin TDO/TDI Is Used to Apply the Test Input Data for JTAG Circuitry

JTAG Fuse Check Mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF} , of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is again taken low after a test or programming session, the fuse check mode and sense currents are terminated.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current flows only when the fuse check mode is active and the TMS pin is in a low state (see [Figure 49](#)). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

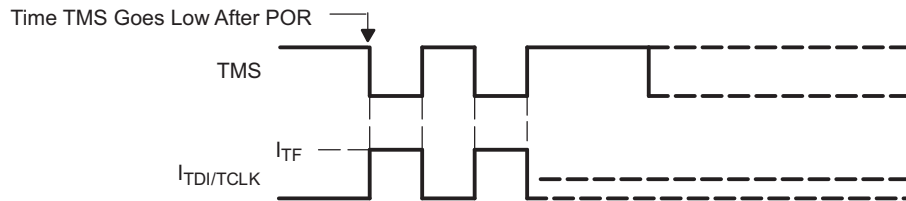


Figure 49. Fuse Check Mode Current

REVISION HISTORY

| LITERATURE NUMBER | DESCRIPTION |
|-------------------|---|
| SLAS541 | Product Preview release |
| SLAS541A | Production Data release Corrected the format and the content shown on the first page. Corrected pin number of P3.6 and P3.7 in 64-pin package in the terminal function list. Corrected the port schematics. Corrected "calibration data" section (page 20). Typos and formatting corrected. Added the figure "typical characteristics - LPM4 current" (Page 33). |
| SLAS541B | Added preview of MSP430F261x BGA devices. |
| SLAS541C | Release to market of MSP430F261x BGA devices |
| SLAS541D | Added the ESD disclaimer (page 1). Added reserved BGA pins to the terminal function list (pages 10 and following). Corrected the references in the output port parameters (page 36). Corrected the cumulative program time of the flash (page 75). |
| SLAS541E | Corrected LFXT1Sx values in Figures 23 and 24 (page 52). Corrected XT2Sx values in Figures 25 and 26 (page 54). Corrected $t_{CMErase}$ MIN value from 200 ms to 20 ms and removed two notes in the flash memory table (page 75). |
| SLAS541F | Renamed Tags Used by the ADC Calibration Tags table to Tags used by the TLV Structure (page 20). Changed value of TAG_ADC12_1 from 0x10 to 0x08 in Tags used by the TLV Structure (page 20). Added CAOUT to P1.0/TACLK, Changed Timer_A3.CCI0A to Timer_A3.CCI1A and Timer_A3.TA0 to Timer_A3.TA1 in P1.2/TA1 row, Changed Timer_A3.CCI0A to Timer_A3.CCI2A and Timer_A3.TA0 to Timer_A3.TA2 in P1.3/TA2 row in Port P1 (P1.0 to P1.7) pin functions table (page 78). Changed TA0 to Timer_A3.CCI0B in P2.2/CAOUT/TA0/CA4 row of Port P2.0, P2.3, P2.4, P2.6 and P2.7 pin functions table (page 80). |
| SLAS541G | Changed limits on $t_{d(SV_{Son})}$ parameter (page 40) |
| SLAS541H | Changed Control Bits/Signals in Table 21 , Table 22 , and Table 23 . Changed crystal signal names in Table 26 and Table 27 . |
| SLAS541I | Changed T_{stg} , Programmed device, to -55°C to 150°C in Absolute Maximum Ratings . |
| SLAS541J | Added nonmagnetic package option to Description and Table 1 . |
| SLAS541K | Changed P8.6/XT2OUT and P8.7/XT2IN to I/O in Table 2 . |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|----------------------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430F2416TPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2416T | Samples |
| MSP430F2416TPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2416T | Samples |
| MSP430F2416TPN | ACTIVE | LQFP | PN | 80 | 119 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2416T | Samples |
| MSP430F2416TPNR | ACTIVE | LQFP | PN | 80 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2416T | Samples |
| MSP430F2416TZQW | ACTIVE | BGA MICROSTAR JUNIOR | ZQW | 113 | 260 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | M430F2416T | Samples |
| MSP430F2416TZQWR | ACTIVE | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | M430F2416T | Samples |
| MSP430F2417TPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2417T | Samples |
| MSP430F2417TPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2417T | Samples |
| MSP430F2417TPN | ACTIVE | LQFP | PN | 80 | 119 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2417T | Samples |
| MSP430F2417TPNR | ACTIVE | LQFP | PN | 80 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2417T | Samples |
| MSP430F2417TZQWR | ACTIVE | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | M430F2417T | Samples |
| MSP430F2418TPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2418T | Samples |
| MSP430F2418TPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2418T | Samples |
| MSP430F2418TPN | ACTIVE | LQFP | PN | 80 | 119 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2418T | Samples |
| MSP430F2418TPNR | ACTIVE | LQFP | PN | 80 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2418T | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|----------------------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430F2418TZQW | ACTIVE | BGA MICROSTAR JUNIOR | ZQW | 113 | 260 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | M430F2418T | Samples |
| MSP430F2418TZQWR | ACTIVE | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | M430F2418T | Samples |
| MSP430F2419TPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2419T | Samples |
| MSP430F2419TPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2419T | Samples |
| MSP430F2419TPN | ACTIVE | LQFP | PN | 80 | 119 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2419T | Samples |
| MSP430F2419TPNR | ACTIVE | LQFP | PN | 80 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2419T | Samples |
| MSP430F2419TZQW | ACTIVE | BGA MICROSTAR JUNIOR | ZQW | 113 | 260 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | M430F2419T | Samples |
| MSP430F2419TZQWR | ACTIVE | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | M430F2419T | Samples |
| MSP430F2616TPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2616T | Samples |
| MSP430F2616TPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2616T | Samples |
| MSP430F2616TPN | ACTIVE | LQFP | PN | 80 | 119 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2616T | Samples |
| MSP430F2616TPNR | ACTIVE | LQFP | PN | 80 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2616T | Samples |
| MSP430F2616TZQW | ACTIVE | BGA MICROSTAR JUNIOR | ZQW | 113 | 260 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | M430F2616T | Samples |
| MSP430F2616TZQWR | ACTIVE | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | M430F2616T | Samples |
| MSP430F2617TPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2617T | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|----------------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430F2617TPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2617T | Samples |
| MSP430F2617TPN | ACTIVE | LQFP | PN | 80 | 119 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2617T | Samples |
| MSP430F2617TPNR | ACTIVE | LQFP | PN | 80 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2617T | Samples |
| MSP430F2617TZQW | ACTIVE | BGA MICROSTAR JUNIOR | ZQW | 113 | 260 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | M430F2617T | Samples |
| MSP430F2617TZQWR | ACTIVE | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | M430F2617T | Samples |
| MSP430F2618TPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2618T | Samples |
| MSP430F2618TPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2618T | Samples |
| MSP430F2618TPN | ACTIVE | LQFP | PN | 80 | 119 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2618T | Samples |
| MSP430F2618TPNR | ACTIVE | LQFP | PN | 80 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2618T | Samples |
| MSP430F2618TZQW | ACTIVE | BGA MICROSTAR JUNIOR | ZQW | 113 | 260 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | M430F2618T | Samples |
| MSP430F2618TZQWR | ACTIVE | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | M430F2618T | Samples |
| MSP430F2619TPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2619T REV # | Samples |
| MSP430F2619TPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2619T REV # | Samples |
| MSP430F2619TPN | ACTIVE | LQFP | PN | 80 | 119 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2619T | Samples |
| MSP430F2619TPNR | ACTIVE | LQFP | PN | 80 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | M430F2619T | Samples |
| MSP430F2619TZQW | ACTIVE | BGA MICROSTAR JUNIOR | ZQW | 113 | 260 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | M430F2619T | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|----------------------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|----------------|
| MSP430F2619TZQWR | ACTIVE | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | M430F2619T | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF MSP430F2618 :

- Enhanced Product: [MSP430F2618-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|----------------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430F2416TPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F2416TPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F2416TPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F2416TZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q1 |
| MSP430F2417TPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F2417TPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F2417TPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F2417TZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q1 |
| MSP430F2418TPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F2418TPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F2418TPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F2418TZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|----------------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430F2419TPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F2419TPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F2419TPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F2419TZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q1 |
| MSP430F2616TPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F2616TPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F2616TPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F2616TZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q1 |
| MSP430F2617TPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F2617TPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F2617TPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F2617TZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q1 |
| MSP430F2618TPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F2618TPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F2618TPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F2618TZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q1 |
| MSP430F2619TPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F2619TPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F2619TPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F2619TZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

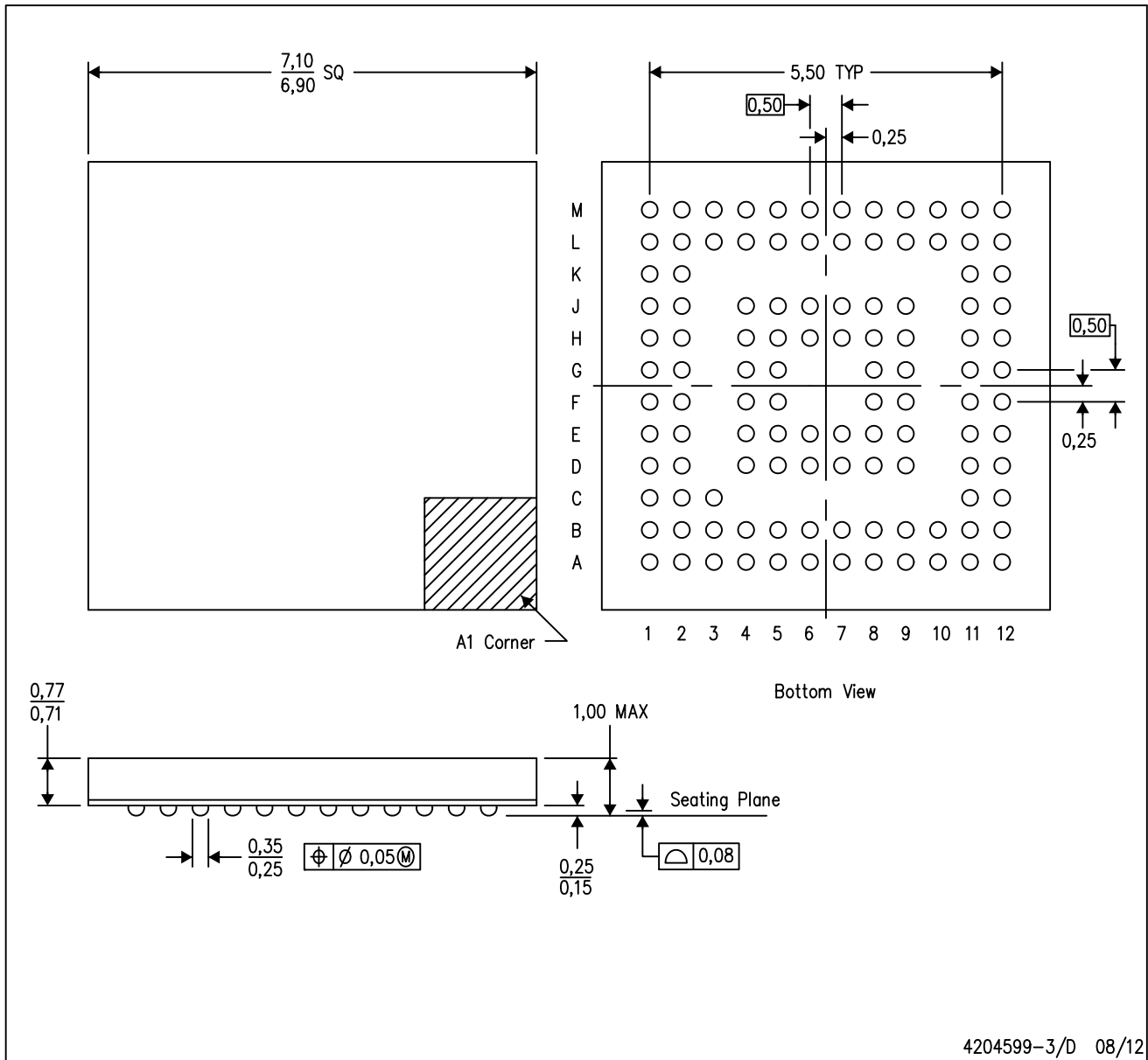

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|----------------------|-----------------|------|------|-------------|------------|-------------|
| MSP430F2416TPMR | LQFP | PM | 64 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F2416TPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| MSP430F2416TPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F2416TZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 350.0 | 350.0 | 43.0 |
| MSP430F2417TPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| MSP430F2417TPMR | LQFP | PM | 64 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F2417TPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F2417TZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 350.0 | 350.0 | 43.0 |
| MSP430F2418TPMR | LQFP | PM | 64 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F2418TPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| MSP430F2418TPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F2418TZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 350.0 | 350.0 | 43.0 |
| MSP430F2419TPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| MSP430F2419TPMR | LQFP | PM | 64 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F2419TPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F2419TZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 350.0 | 350.0 | 43.0 |
| MSP430F2616TPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| MSP430F2616TPMR | LQFP | PM | 64 | 1000 | 350.0 | 350.0 | 43.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|----------------------|-----------------|------|------|-------------|------------|-------------|
| MSP430F2616TPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F2616TZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 350.0 | 350.0 | 43.0 |
| MSP430F2617TPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| MSP430F2617TPMR | LQFP | PM | 64 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F2617TPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F2617TZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 350.0 | 350.0 | 43.0 |
| MSP430F2618TPMR | LQFP | PM | 64 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F2618TPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| MSP430F2618TPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F2618TZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 350.0 | 350.0 | 43.0 |
| MSP430F2619TPMR | LQFP | PM | 64 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F2619TPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| MSP430F2619TPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F2619TZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 350.0 | 350.0 | 43.0 |

ZQW (S-PBGA-N113)

PLASTIC BALL GRID ARRAY



MicroStar Junior is a trademark of Texas Instruments.

PN (S-PQFP-G80)

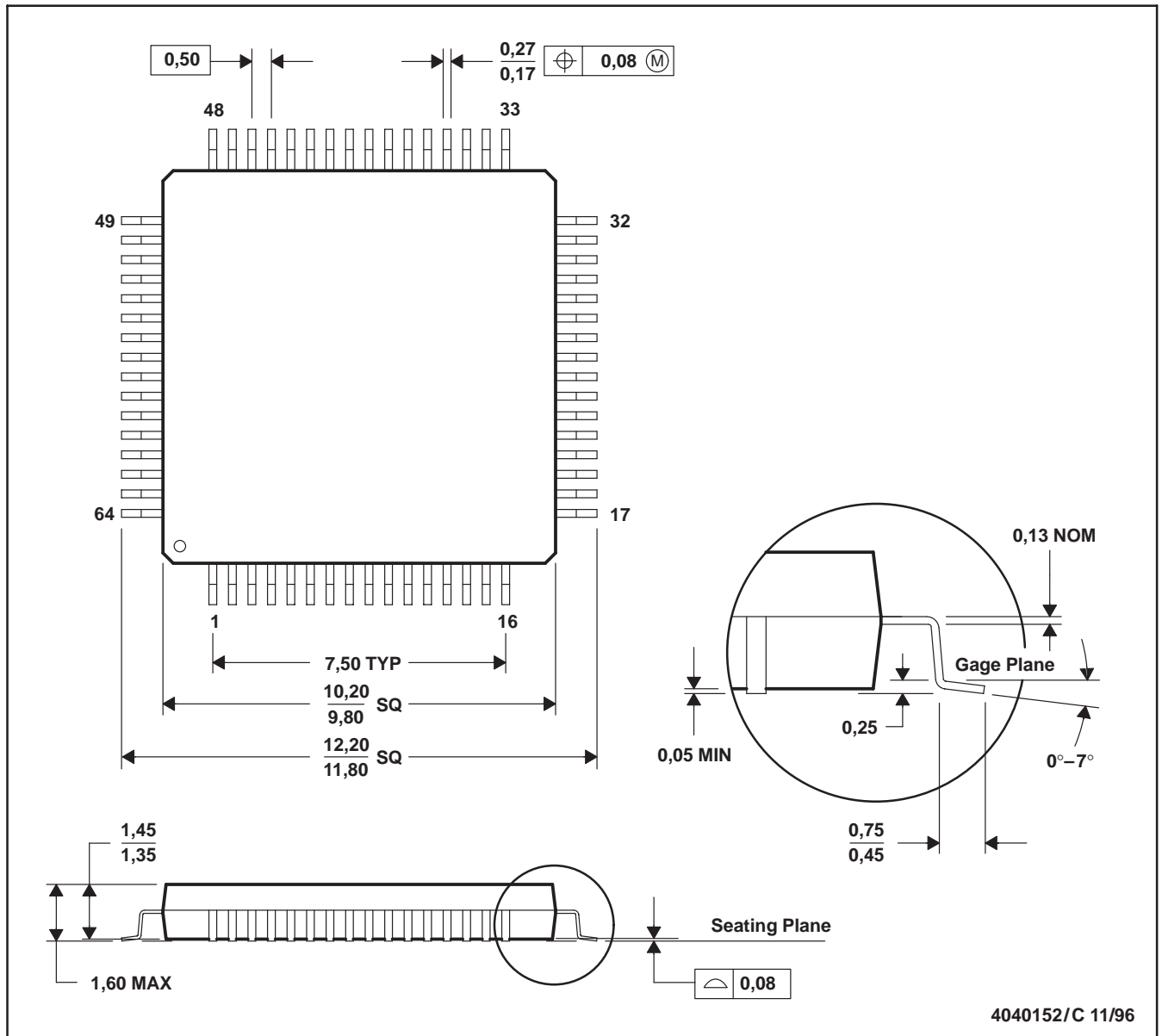
PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

PM (S-PQFP-G64)

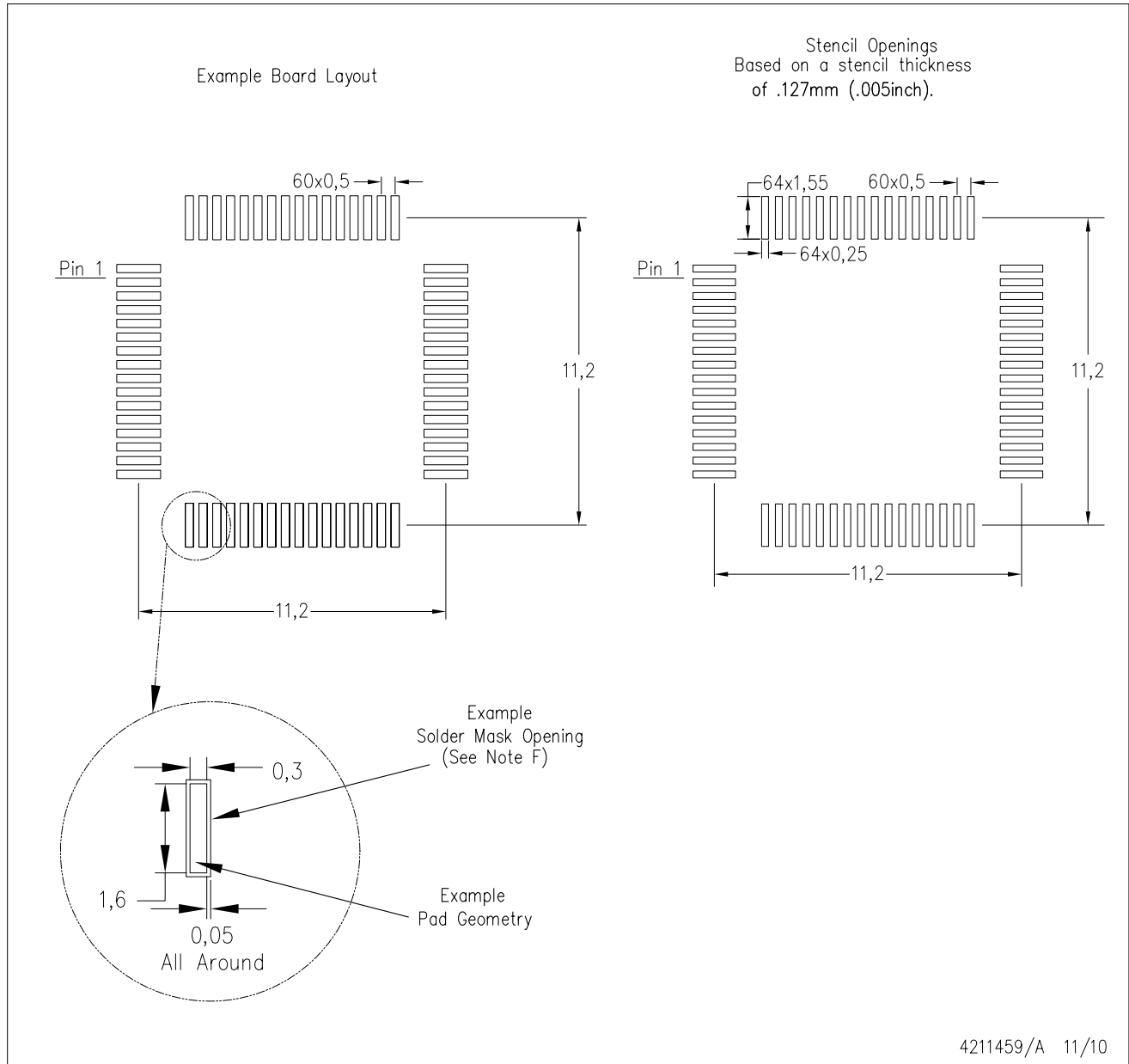
PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026
 D. May also be thermally enhanced plastic with leads connected to the die pads.

PM (S-PQFP-G64)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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